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NASA Contractor Report 3323

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Satellite Power Systems (SPS) Concept Definition Study

Volume VI - In-Depth Element Investigation

G. M. Hanley

CONTRACT NAS8-32475
SEPTEMBER 1980

NASA

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NASA Contractor Report 3323

Satellite Power Systems (SPS) Concept Definition Study

Volume VI - In-Depth Element Investigation

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Rockwell International
Downey, California

Prepared for
Marshall Space Flight Center
under Contract NAS8-32475

National Aeronautics
and Space Administration

**Scientific and Technical
Information Branch**

1980

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FOREWORD

This is Volume VI - *In-Depth Element Investigations*, of the SPS Concept Definition Study Final report as submitted by Rockwell International through the Satellite Systems Division. All work was completed in response to the NASA/MSFC Contract NAS8-32475, Exhibit C, dated March 28, 1978.

The SPS final report will provide the NASA with additional information on the selection of a viable SPS concept and will furnish a basis for subsequent technology advancement and verification activities. Other volumes of the final report are listed as follows:

Volume	Title
I	Executive Summary
II	Systems Engineering
III	Experimentation/Verification Element Definition
IV	Transportation Analyses
V	Special Emphasis Studies
VII	Systems/Subsystems Requirements Data Book

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1.0 INTRODUCTION

1.0 INTRODUCTION

The Department of Energy (DOE) is currently conducting an evaluation of approaches to provide energy that will meet demands in the post-2000 time period. The Satellite Power System (SPS) is a candidate for producing significant quantities of base-load power using solar energy as the source.

The SPS concept is illustrated in Figure 1.0-1 for a solar photovoltaic concept. A satellite, located at geosynchronous orbit, converts solar energy to dc electrical energy using large solar arrays. The dc electrical energy is conducted from the solar arrays to a microwave antenna. At the microwave antenna, the dc energy is transformed to microwave RF energy. A large, 1-km-diameter antenna beams the energy to a receiving antenna (rectenna) on the ground. The rectenna converts the RF energy, at very high efficiency, to dc electrical energy which is input to the utility network for distribution.

Typically, a single SPS provides 5 GW of power to the utility interface on the ground. Two satellite power systems would provide more power than is needed by large metropolitan areas such as Los Angeles, New York, or Chicago. Because of the large dimensions of the satellite (the solar array area is approximately 75 km^2) and the large mass (approximately 35 million kg), it is necessary to construct the satellite on orbit where zero-gravity allows

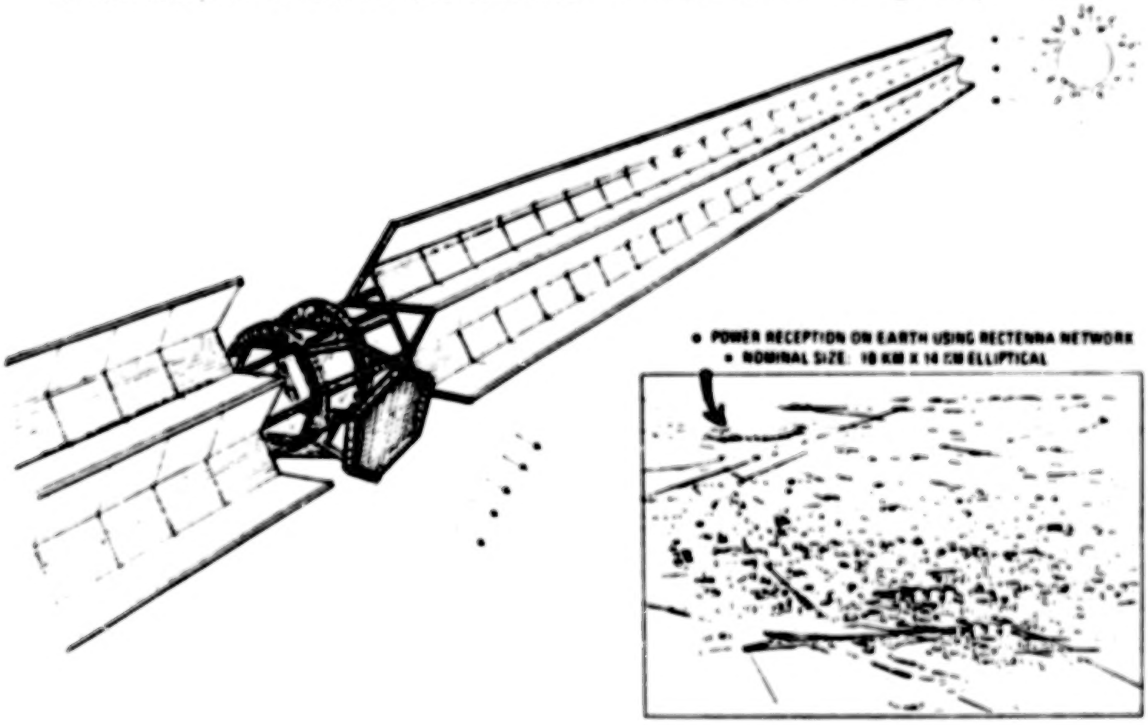

Figure 1.0-1. Satellite Power System Concept

very low structural mass. The ground-located rectenna is nominally an elliptical array 10 km by 13 km. At the earth's surface, the microwave beam has a maximum intensity in the center of 23 mW/cm^2 (less than one-fourth the solar constant), and an intensity of less than 1 mW/cm^2 outside of the rectenna fenceline (10 mW/cm^2 is the current U.S. microwave exposure standard).

The data discussed in this volume form part of a continuing study effort to provide system supportive definition data to aid in the evaluation of the SPS concept (by DOE). The specific area of evaluation discussed is relative to the use of a conceptual solid-state alternative to microwave transmission

The following sections present a summary of the study activities, the specific task objectives, the study statement of work, and a summary of the study results and conclusions. The complete, detailed study report including appropriate computer printouts is included in the appendix.

1.1 STUDY APPROACH

An overview of the overall study approach logic, reflecting a two-phase emphasis of the study, is shown in Figure 1.1-1. In the first phase, major consideration is given to refining, adding substantiation to, and updating the SPS point design to support the baseline con ept selection. In the figure, only the flow paths of the most significantly in luencing outputs between subtasks are shown. As noted by the flow path lines, Subtask 5.1 (Systems Engineering), encompassing the point design update, is the ultimate recipient of the major subtask outputs for this phase.

The second phase of the study concentrated on the development of program plans based on a selected baseline concept(s).

This document addresses only those activities associated with Task 1.0, In-Depth Element Investigations. The hardware device selected for detailed analysis is the solid-state transistor and its applicability to microwave power transmission.

1.2 OBJECTIVE

The objective of this task was to conduct an in-depth investigation of a specific hardware element that may have potential for major system cost savings.

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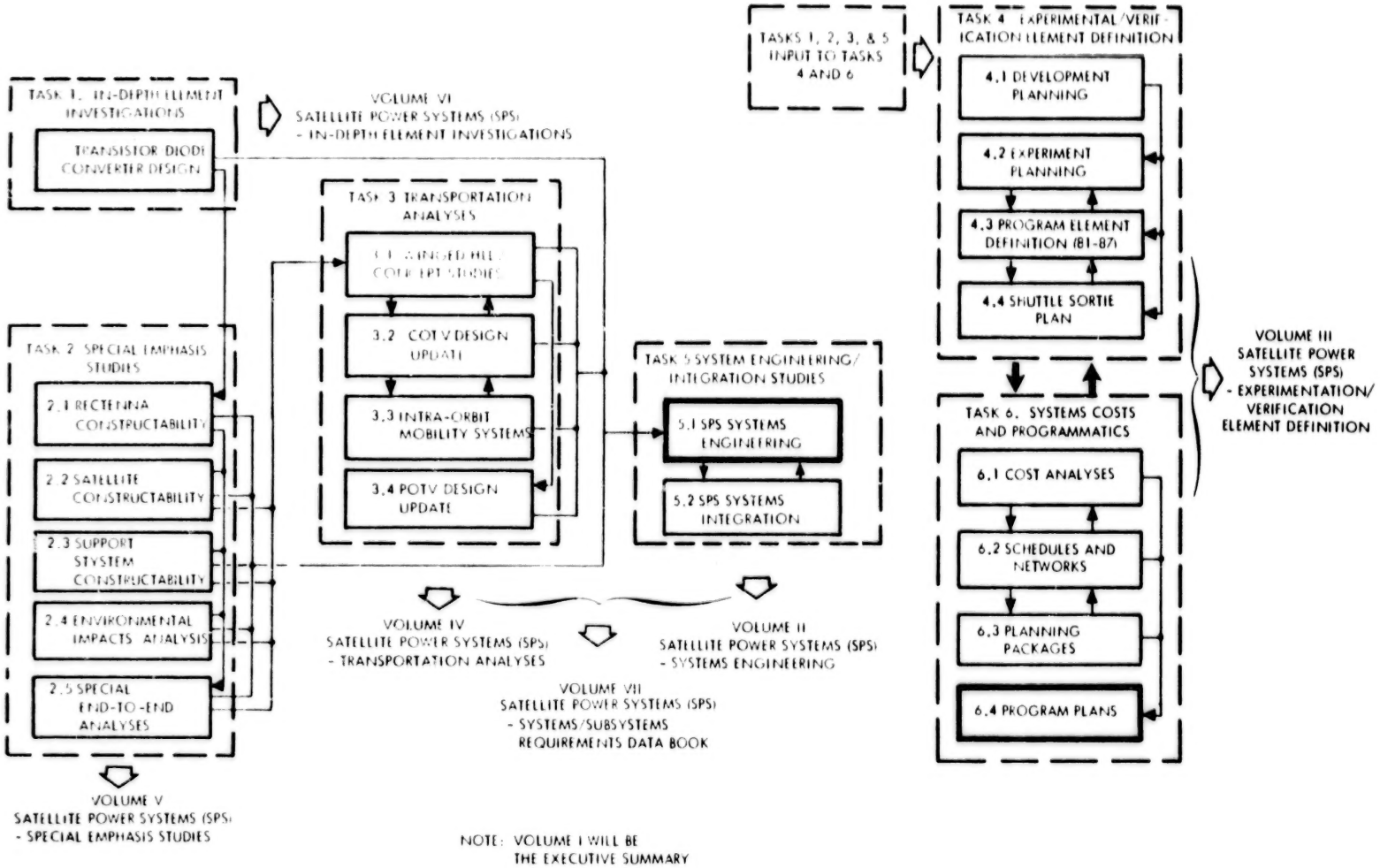
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TRANSISTOR DIODE CONVERTER DESIGN
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VOLUME V
SATELLITE POWER SYSTEMS (SPS)
- SPECIAL EMPHASIS STUDIES
NOTE: VOLUME I WILL BE THE EXECUTIVE SUMMARY

Figure 1.1-1. Study Logic Overview

2.0 STUDY TASK DESCRIPTION

2.0 STUDY TASK DESCRIPTION

2.1 INTRODUCTION

The specific task involved the performance of key in-depth, low-cost exploratory technology investigations and laboratory experimentation of specific SPS hardware elements that have the potential to provide major early cost saving, performance improvement, or critical issue resolution. The tasks and depth of experimentation were substantially constrained by the available funding allocations.

A single high-priority task was identified for investigation: *Computer-assisted design of a gallium arsenide solid-state dc-to-RF converter with supportive fabrication data.*

A number of alternatives was considered including: GaAs solar cell fabrication techniques, basic array radiating element resonant cavity radiator (RCR), and stripline bow-tie dipole antenna elements.

The gallium-arsenide, solid-state, dc-to-RF converter investigation was selected since it offers a simplified alternative to klystron tubes provided that high enough efficiencies can be achieved and the structure of an optimum transistor can be designed and mass fabricated. This design would offer potential resolutions to key issues in power transmission of element life/failure rates/maintenance.

The computer simulation effort on the theoretical efficiencies of microwave transistors, performed by the University of Waterloo (Dr. David Roulston) under subcontract to Rockwell in the previous SPS study (NAS8-32475, Exhibits A and B), showed much promise.

Transistor converters are attractive for dc-RF conversion because they are solid state and produce a simple cooling structure. It appears that GaAs transistors can achieve efficiencies high enough to be competitive with klystrons. If such efficiencies can be achieved, design of the microwave antenna may be simplified and system reliability greatly enhanced. Design effort was not complete enough at that time to give the structure of an optimum transistor or predict its detailed performance; nor can technical risk be estimated at this time. Table 2.1-1 provides a summary of the results of the power transistor study.

To incorporate GaAs transistor and diode power converters into the MPTS point design, several optimum device and circuit designs were investigated. Drs. D. Roulston, I. Hajj, and P. Bryant of Waterloo University utilized existing programs for the computer-aided design of semiconductor devices and their associated circuits, while Rockwell used REDAC, a nonlinear circuit computer program. Rockwell supplied data on the parameters characterizing GaAs as a semiconductor for Dr. Roulston's device program.

Table 2.1-1. Summary of Initial Power Transistor Data

Amplifier Requirement

Frequency = 2.45 GHz
Load resistance = 70 ohms
Power = 120 watts

Push-Pull Class E Amplifier Analytic Results by Wiley (Rockwell)

Material	Gain Est.	Collector Eff.	Amplifier Eff.
Silicon	10 dB	46%	36%
Gallium arsenide	13 dB	83%	78%

Class C Amplifier Computer Results by Roulston (Univ. of Waterloo), Silicon Transistor

Mode	Power	Gain	Collector Eff.	Amplifier Eff.
Single-end	22.3 W	8.6 dB	81%	67%

Comparison with Experimental Class C Results (TRW Model RD-2040-6, G = 9 dB)

Mode	Power	Collector Eff.
C Single-Ended	40 W	55%
C Single-Ended	120 W	10%
C Push-Pull	120 W	41%

It was the intent of this task to produce a solid-state device design that could be incorporated into a conceptual satellite system design. It was expected that use of solid-state converters would have significant impact on the SPS configuration in such areas as antenna size, power distribution design, and thermal/structural design. It must be pointed out that the question of feasibility of fabricating the device cannot be answered within the constraints of this study. Although it is not anticipated that this study would provide recommended changes to the current design by the DOE need date (September 1978), it was suggested that it be performed for recommended "downstream" design changes.

2.2 STATEMENT OF WORK

Four specific activities were identified in this study: Computer Program Checkout, Amplifier Comparisons, Computer Design, and GaAs Diode Evaluation.

Computer Program Checkout—Check out existing programs for the computer-aided design of transistor devices and their associated circuits. This will be done by comparing experimental amplifier results for silicon transistors with computer predictions.

Amplifier Comparisons—Compare Class C and Class E amplifier types. Class E amplifier test data from MSFC will be integrated into this comparison as it becomes available. A best amplifier type will be selected on the basis of results of the comparison.

Computer Design—Compile GaAs parameters for use in computer design analysis. Existing gallium-arsenide solar cell material parameters will be utilized where appropriate, e.g., diffusion lengths, lifetimes, etc. Parameters will be experimentally derived when necessary to supplement existing data. Carry out computer-aided design of a GaAs power transistor, along with related circuit design and obtain an optimum design based on performance.

GaAs Diode Evaluation—Evaluate GaAs diode designs. Select five diode designs for comparison, each at a different design power level.

3.0 INVESTIGATION SUMMARY

3.0 INVESTIGATION SUMMARY

The results obtained in the design and evaluation of transistors for Class C and Class E amplifier candidates proposed for the microwave power transmission system (MPTS) in the Satellite Power System (SPS) are described in this section. The goal for this study was the determination of transistor fabrication parameters suitable for power conversion efficiencies of at least 80 percent, with power gains of at least 10 dB, and verification of the chosen devices using suitable modeling and computer simulation (Reference 1). Initially, a frequency of 915 MHz was chosen for the output power; however, in subsequent phases the effort was concentrated on a 2.45-GHz device and circuit.

3.1 CLASS C AMPLIFIER

In the Class C amplifier (Reference 2), the quiescent point is chosen so that the collector current flows for less than one-half cycle. Efficiency (η_c) of the Class C amplifier is given by the following (see Figure 1.1-1):

$$\eta = \frac{\text{ac power delivered to the load at the fundamental frequency}}{\text{dc power supplied by the collector supply}} .$$

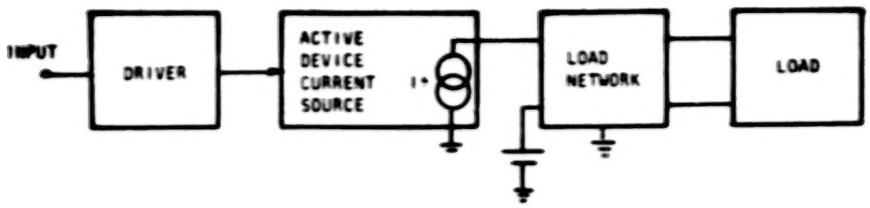
If the conduction angle (θ) is small:

$$\eta_c = \left(1 - \frac{V_{ce\ min}}{V_{cc}}\right), \qquad (1)$$

where $V_{ce\ min}$ is the minimum instantaneous voltage at the collector and V_{cc} is the collector supply voltage. $V_{ce\ min}$ is limited by the collector resistance R_c and the instantaneous collector current. Also, η_c can be expressed as a function of conduction angle:

$$\eta_c = \frac{\theta - \sin\theta}{4 \sin\theta/2 - 2\theta \cos\theta/2} . \qquad (2)$$

An ideal Class C amplifier has 100 percent efficiency for zero conduction angle, but total power delivered to the load is zero for this condition. The high efficiency of the Class C amplifier is due to the fact that the collector current is not allowed to flow except when the instantaneous collector voltage is low (ideally zero), i.e., the collector supply V_{cc} supplies energy to the amplifier only when the largest portion of this energy will be absorbed by the load network. The smaller the fraction of the cycle during which collector current flows, the greater will be the efficiency.



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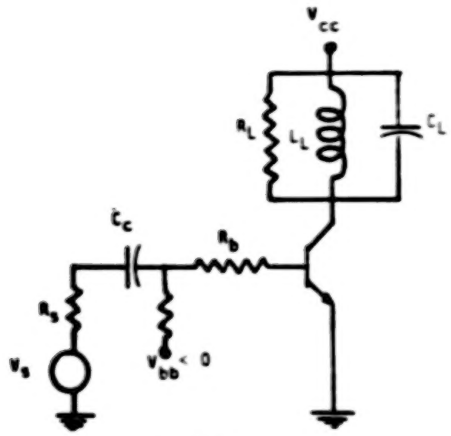
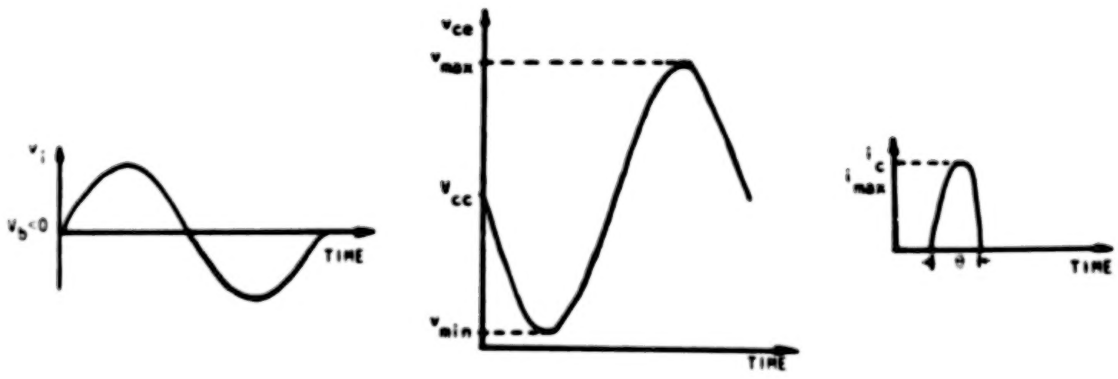


CIRCUIT



WAVESHAPES

Figure 3.1-1. Single-Ended Class C Amplifier

Figure 3.1-1 shows the block diagram of a Class C tuned amplifier. The active device, in a Class C amplifier, acts as a high impedance current source when appropriately driven by the driver. The output current is determined by the input drive and is assumed to be independent of the output voltage which results from the flow of current in the load network (the load is usually resistive).

3.2 CLASS E AMPLIFIER

As pointed out in Class C operation, the active device has sufficient minimum voltage across it when conducting to prevent saturation of the active device; this is necessary to keep the design assumptions valid. Thus, in the Class C amplifier, there is always power dissipation in the active device, which means reduced efficiency.

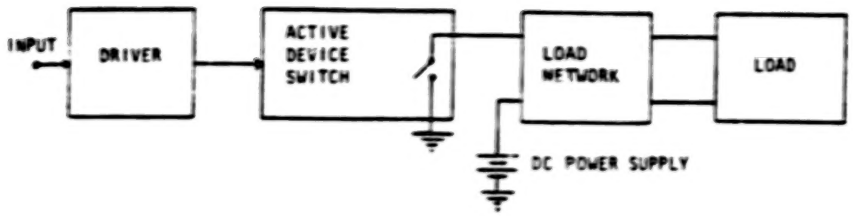
The Class E concept (References 3 and 4) offers a new means of producing highly efficient power amplification. In Class E operation, the active device acts as a time-varying admittance (Reference 5) and is used as a switch. In the optimum case of a Class E amplifier, the voltage across the device is nearly zero when it is on, i.e., the current is flowing through it; and the current through the dvice is zero when it is off, i.e., very small power is dissipated in the device.

Figure 3.2-1 shows the block diagram and a simple circuit of single-ended Class E amplifier.

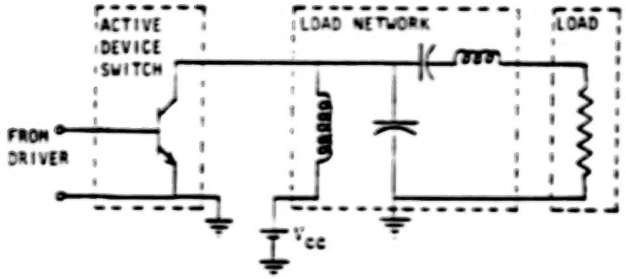
The load network is a very critical element of the Class E amplifier. The load network is designed so that it gives a steady-state response which avoids any duration of time in which appreciable current through and voltage across the active device exist simultaneously. This condition is achieved if the device switching times (turn-on and turn-off) are an appreciable fraction of the ac cycle. The load network may include a lowpass or bandpass filter to suppress harmonics of the switching frequency at the load. It may also transform the load impedance and accommodate load reactance.

The load can either be a lumped impedance or distributed impedance of a transmission line or waveguide.

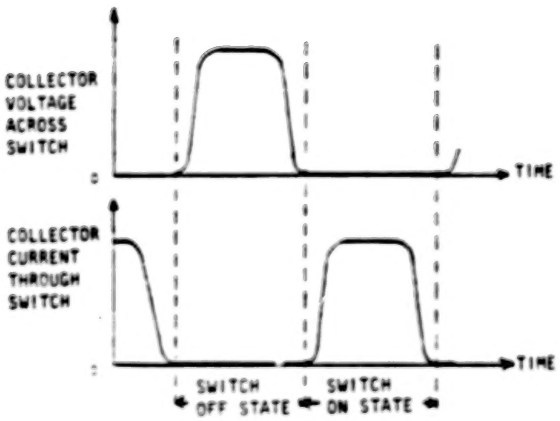
Figure 3.2-1 also shows the desired ideal waveforms of voltage across the switch and current through the switch in a Class E amplifier circuit for maximum efficiency of operation.



BLOCK DIAGRAM



CIRCUIT



WAVESHAPES

Figure 3.1-1. Single-Ended Switching Mode Class E Amplifier

3.3 AMPLIFIER CIRCUIT DESIGN RESULTS

Different transistors were designed and studied in Class C amplifier circuits at two different operating frequencies—914 MHz and 2.45 GHz. In this report, the detailed discussion to the transistor and circuit performance is limited to 2.45 GHz. The results of the performance of two transistors are shown; one is a silicon transistor and the other is a gallium-arsenide transistor.

The performance of the transistor in a Class C amplifier circuit was evaluated with WATAND using the BIPOLE-generated extended Ebers-Moll model (Reference 1).

Figure 3.3-1 shows the efficiency versus gain (η vs. G_p) curves for the silicon transistor in saturated Class C and Class E configurations at a power output level of about 11 watts. Note that for low-power gain (<13) the performance of the transistor in the Class C configuration is better than its performance in the Class E configuration, and vice versa when $G_p > 13$.

However, at a higher output power level of approximately 20 watts, the performance of the silicon transistor in the saturated Class C amplifier circuit configuration is better than its performance in a Class E configuration (Figure 3.3-2), indicating that the Class C amplifier might perform better than the Class E amplifier at certain higher output power levels.

Also, preliminary results indicate that the Class E amplifier configuration is much more sensitive to parameter variations compared with the Class C amplifier. A one-percent to four-percent variation in certain reactive elements can cause up to 3-dB gain variations in the Class E amplifier configuration.

In addition, Figures 3.3-3 and 3.3-4 show the performance of the silicon and GaAs transistors with temperature as a parameter. It is evident that the silicon transistor performance is generally best at low temperatures (27°C) and the GaAs transistor performance is best at higher temperatures (100°C to 150°C).

A more detailed description of the results of this investigation is included in the appendix.

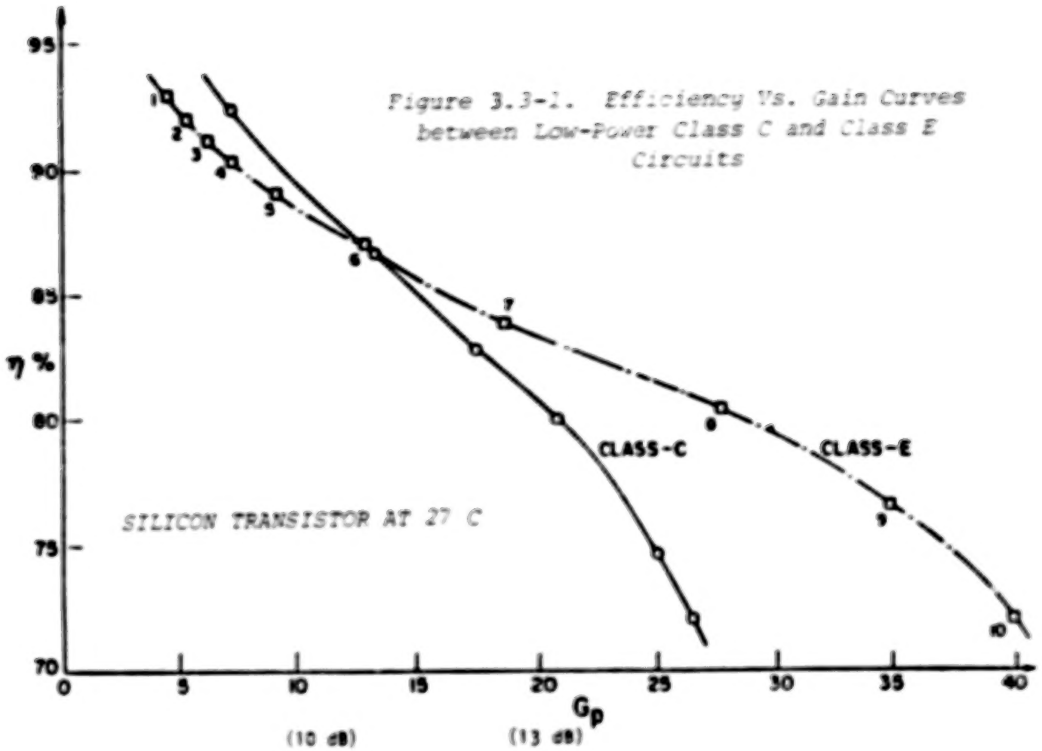


Figure 3.3-1. Efficiency Vs. Gain Curves between Low-Power Class C and Class E Circuits

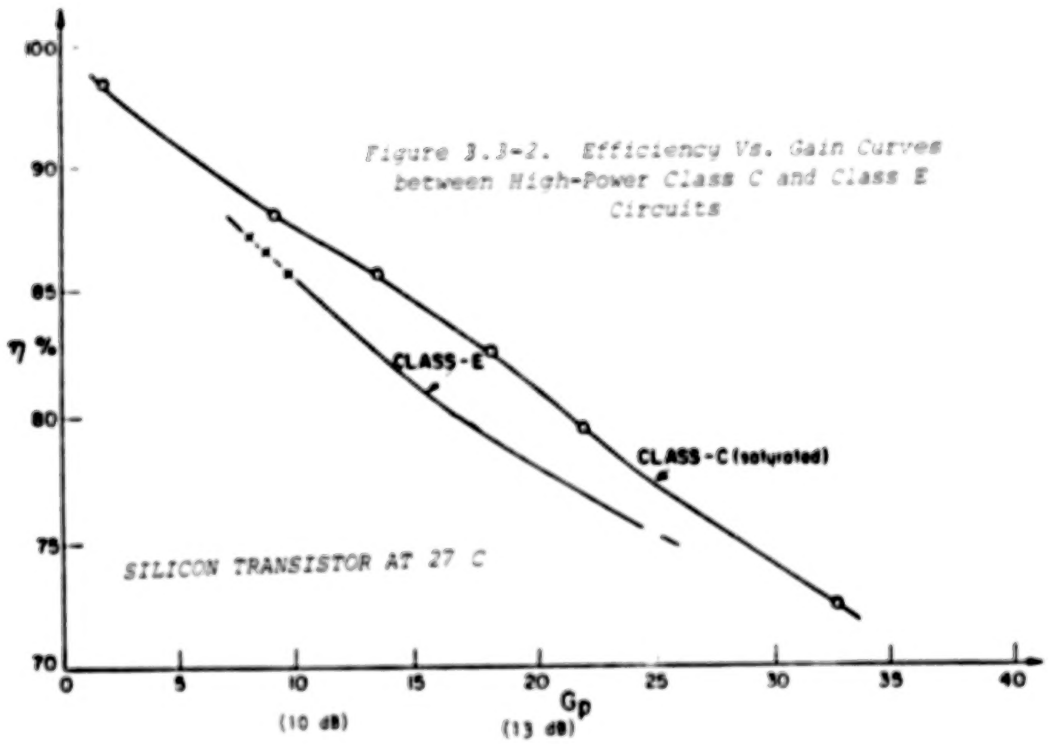


Figure 3.3-2. Efficiency Vs. Gain Curves between High-Power Class C and Class E Circuits

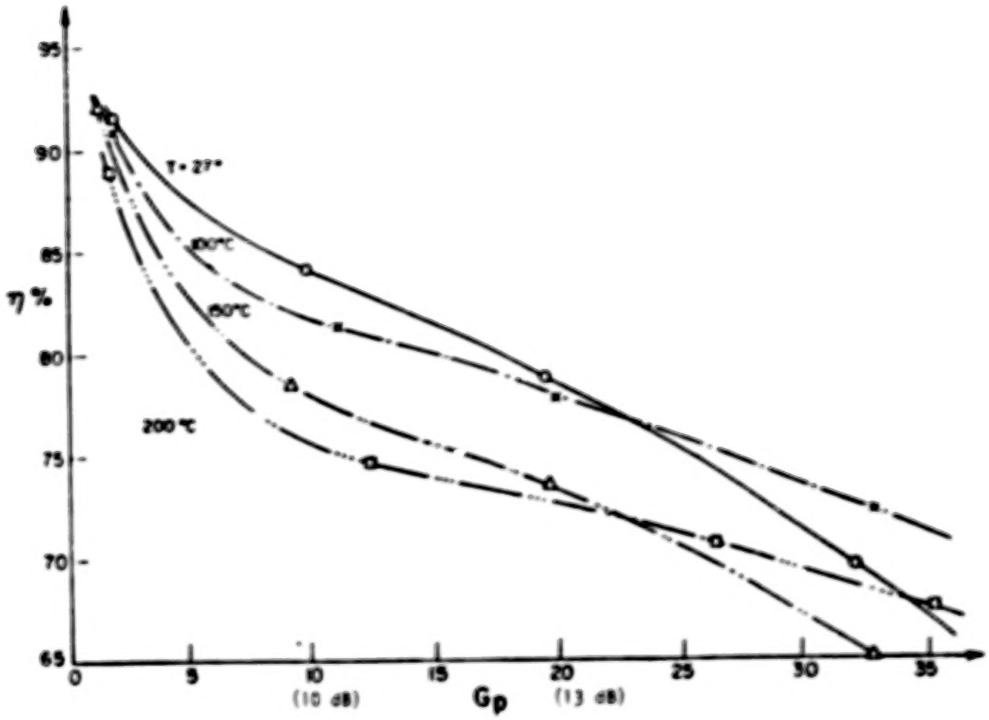


Figure 3.3-3. Silicon Transistor at Various Operating Temperatures

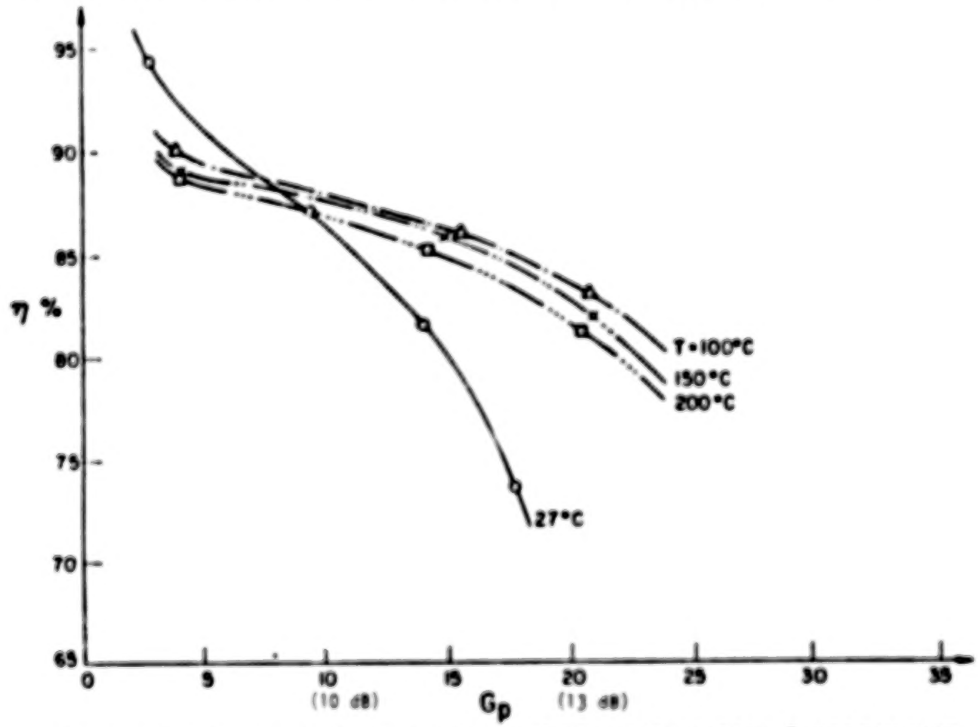


Figure 3.3-4. GaAs Transistor at Various Operating Temperatures

3.4 REFERENCES

1. D. J. Roulston, I. N. Hajj, and P. R. Bryant, *Design and Evaluation of High Efficiency Si and GaAs Bipolar Transistors and of their Performance in Class C and E Circuits used for Microwave Transmission in the Satellite Power System*, prepared for Rockwell International, WRI Project 707-12-02 by University of Waterloo, Waterloo, Ontario, Canada, December, 1978.

2. N. Goel, *Study of Non-Linear Power Amplifiers, with Special Emphasis on Class E Circuits, using WATAND*, M.S. Thesis, Tech. Report No. UW EE 78-6, University of Waterloo, Waterloo, Ontario, Canada, August, 1978.

3. N. O. Sokal and A. D. Sokal, *Class E—A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers*, IEEE Journal of Solid-State Circuits, pp. 168-175, June, 1975.

4. F. H. Raab, *Effects of Circuit Variations on the Class E Tuned Power Amplifier*, IEEE Journal of Solid-State Circuits, pp. 239-246, April, 1978.

5. L. A. Wilson, *High-Frequency Transistor Power Amplifiers*, Ph.D Dissertation, UCLA, Los Angeles, California, 1973.

APPENDIX

SOLID-STATE MICROWAVE TRANSMISSION SYSTEM DESIGN AND EVALUATION

Note: This investigation was conducted at the University of Waterloo, Ontario, Canada by D. J. Roulston, I. N. Hajj, and P. R. Bryant. This effort was performed for Rockwell International, Satellite Sustems Division, Seal Beach, CA, under Agreement for Services No. M8M8BNS-892055E as part of the Satellite Power Systems (SPS) Concept Definition Study, Exhibit C, contract with NASA/MSFC.

1. Introduction

In this report we describe the results obtained in the design and evaluation of transistors for the microwave space power system. The goal for this study was the determination of transistor fabrication parameters suitable for power conversion efficiencies of at least 80% with power gains of at least 10 dB and verification of the chosen devices using suitable modeling and computer simulation. Initially, a frequency of 915 MHz was chosen for the output power, however, in the subsequent phases of the contract our effort was concentrated on a 2.45 GHz device and circuit as requested by the terms of the contract.

Following this introduction the report is divided into seven major sections:

Section

2 - outline of the procedure used for 'roughing out' the transistor fabrication data and
presentation of the performance data obtained using the BIPOLE computer program, for both Silicon and Gallium Arsenide transistors.

3 - discussion of the non-linear CAD transistor models generated by the BIPOLE program and their evaluation using WATAND and low frequency laboratory experiments.

4 - description of the method used to obtain the performance of the transistor in a class C amplifier configuration using the WATAND computer program and presentation of the results obtained at both frequencies, for both Silicon and Gallium Arsenide transistors.

5 - presentation of the results obtained for the class E amplifier configuration for the silicon transistor.

6 - comparison of efficiency versus power gain curves for different junction temperatures and with various parasitic effects included (for class C).

7 - preliminary fabrication data and circuit evaluation using WATAND for eight diodes for use in the ground rectenna system.

To avoid undue repetition of results presented in previous reports, a number of appendices are attached; these summarize parts of the theoretical study and include some of the intermediate results.

Section 8 presents a brief summary of the overall results, including conclusions concerning class C versus class E, 915 MHz versus 2.45 GHz operation, limitations of the modeling technique used, temperature considerations.

2. Transistor Design

2.1 Summary of Analytic Method

Reference [1] gives a detailed description of the analytic and computer simulation methods used to obtain a bipolar transistor design, for a specified power conversion efficiency and power gain at a given frequency. Let us recall here the basic features of the approach used.

A fundamental parameter for high frequency operation is the power gain, conveniently expressed as:

$$G_p = (f_{mosc}/f_s)^2 \tag{1}$$

Where f_{mosc} is the maximum oscillation frequency of the device and f_s the signal frequency. Using the well established relationship (deduced from the small signal parameters in terms of physical device parameters [1], as shown by the summary in Appendix 1.1, gives:

$$f_{mosc} = (1/L)\sqrt{(3V_{th}/4\pi\varepsilon)\ (D_n/V_{th})^{1/2}\ \sigma_b\ W_{scl}}^{1/2} \tag{2}$$

where
- L is emitter stripe width
- σ_b is the active base region conductivity
- W_{scl} is the collector-base space charge layer width
- V_{th} is the saturated drift velocity of electrons
- D_n is the electron diffusion constant in the base
- ε is the permittivity

This expression (2) assumes an optimised structure in which the neutral base and c-b space charge layer transit times have been set equal. Even though, in class C operation, the gain will be different from that given by (1), due to output mismatch (the load for maximum power gain is, in general, not the same as for maximum power conversion efficiency), it is intuitively obvious that a high value of f_{mosc} is necessary. Equation (2) tells us that in order to increase f_{mosc}, W_{scl} must be increased. This implies a lower

collector doping and higher breakdown voltage. The f_t would be decreased. This brings to light the limitation of (1) and (2). They are, in fact, only valid for $f_s \leq f_t$, the transition frequency.

We can conclude from the above discussion, that in order to improve the high frequency power gain, the emitter stripe width L, must be reduced as far as technologically possible, and W_{scl} (and thus the c-b breakdown voltage) must be kept as high as possible consistent with the condition:

$$f_s \leq f_t \tag{3}$$

$$f_t \approx V_{th}/(2\pi W_{scl}) \tag{4}$$

Clearly, the base conductivity σ_b must be kept as high as possible. This is limited finally by current gain $h_{FE} \approx h_{fe}$, such that the condition:

$$h_{FE} \geq f_t/f_s \tag{5}$$

is satisfied.

The maximum collector current is limited by the Kirk effect to approximately:

$$I_k = qBLV_{th} N_{epi} \tag{6}$$

where q is the electronic charge, B the total emitter stripe length and N_{epi} the collector doping level. The maximum value of base-collector breakdown voltage is:

$$V_{cbr} = F_{vc} \varepsilon E_{br}^2/(2q N_{epi}) \tag{7}$$

where F_{vc} is a constant of order 0.5 to 1.0 depending on fabrication (planar, moat etch, etc.), and E_{br} (the maximum field at breakdown), is a slowly varying function of N_{epi}.

Since the load resistance for maximum class A power output will be:

$$R_{Lm} = V_{cbr}/I_k \qquad (8)$$

it is clear that we have a set of relations which can be used to determine at least initial values for the device parameters. These relations are summarized in Appendix 1.2. In order to estimate the parameters for class C operation, we have, as discussed in [1] and summarized in Appendix 1.3, defined the following additional parameters:

η_V (ETAV): the low frequency voltage efficiency

η_I (ETAI): the low frequency current efficiency

η (ETA): the overall low frequency efficiency

η_F (ETA(F)): the high frequency efficiency including R_c (collector series resistance) loss

η_ν (ETANU): the high frequency efficiency including estimated input switching time loss

η_o (ETAD): the overall high frequency efficiency

In addition, the class C high frequency power gain GDBNU, using empirically estimated relations, has been calculated.

2.2 Analytic Results at 2.45 GHz

A sample of the results based on the above equations is tabulated in Appendix 2 in the form of computer output, for a signal frequency of 2.45 GHz. This page corresponds to a conduction angle of 100° and an initial power gain of 20. The value of f_t (FT (REAL)) is varied from f_s to $8f_s$. For each value of f_t the corresponding values of breakdown voltage (VCBR), base width (WB) f_{mosc} (FMO), etc. are printed. Then follows, for each successive f_t, calculated results for emitter stripe widths (ELEM) varying from 1um to 4um. The estimated values of power gain in dB (GDBNU) and overall efficiency (ETAO) are printed for each stripe width.

From the complete set of tables given in [2], we have obtained the curves shown in Fig. 1(a) and (b) of power conversion efficiency versus conduction angle for two emitter stripe widths and a range of f_t values. For each value of f_t we have listed the corresponding value of collector-base breakdown

voltage V_{cbr}. It can be seen that we must have a conduction angle between 100^{o} and 160^{o} with the optimum value depending on the emitter stripe width and f_t value.

For Silicon, it is seen that to obtain 80% efficiencies, we must have a stripe width of (at most) 2 microns with an f_t of 20 GHz (a breakdown voltage, V_{cbr} of 16 volts), or a 1 micron stripe width with f_t of about 6 GHz (V_{cbr} about 35 volts).

For Gallium Arsenide it is seen (Fig. 1 (b)) that the 80% efficiency can be comfortably exceeded with a stripe width of 2 microns and f_t = 2.5 GHz (V_{cbr} = 77 volts) and that using a stripe width of 1 micron should yield efficiencies close to 90% with V_{cbr} about 40 volts.

The results of this study are of course, very approximate, particularly for power gain estimation and give no detailed information about impurity profiles. They were used to determine initial "guesses" for device data as input to the BIPOLE program.

2.3 Detailed Study of D.C. and Small Signal H.F. Parameters from Impurity Profile Data Using Bipole.

The theoretical basis behind the BIPOLE program has been fully reported in the literature [13, 14, 15, 16]. We shall simply recall here, that the program divides the device into space charge and neutral regions, (5 regions from emitter contact to collector contact). The boundaries of these regions are current-density and voltage dependent. This is the so-called "variable-boundary regional" approach. For each region, the transport equation, or Poisson's equation, is numerically integrated and iterations effected until the defined boundary conditions are satisfied. Doping level mobility dependence, velocity versus electric field dependence, and high doping band gap reduction effects are included in the program. Its formulation implicitly includes all known high level effects such as conductivity modulation, base widening, quasi-saturation. The terminal characteristics are derived by combining the vertical (e-b-c) integration results with a horizontal integration of the base transport equation. From the numerical analysis, terminal d.c. characteristics and capacitance values, plus small signal parameters such as the transition frequency f_t and the maximum oscillation frequency f_{mosc} are

computed. The input to the BIPOLE program consists of impurity profile and lifetimes plus geometry data.

The program is extremely rapid; a run giving a condensed set of output characteristics (including f_t and f_{mosc} versus I_c) requires an execution time of about 5 seconds on the IBM 370/158 computer on CMS. Using a high speed line and a Tektronix graphics terminal, it is possible to study ten or more designs in a one hour session at the terminal. When a promising looking set of characteristics is obtained, a complete output is generated and examined and a circuit model is stored on disc to be accessed by the WATAND program.

In Appendix 3, we reproduce the complete BIPOLE output for the final 2.45 GHz Silicon transistor, plus a summary discussion of the output data. The output for the other transistors was included in [1,2]. Fig. 2(a, b, c) gives the impurity profiles for the three transistors finally used, SP9S1, the 915 MHz Silicon device, SP2S2, the 2.45 GHz silicon device and SP2A2, the 2.45 GHz Gallium Arsenide device. These profiles are as generated by the BIPOLE program. A complete list of the basic data for each of the three transistors is shown in Table 1. Note the use of an ion implanted base in the Silicon device to improve the performance by increasing the active base region conductivity. In the Gallium Arsenide device, the emitter has relatively light doping. This was done because (a) it has been suggested elsewhere [24] that increased doping would not improve the h_{FE}, (b) little information was found in the literature concerning high doping band-gap reduction effects in Gallium Arsenide, so the use of higher doping levels would have produced unreliable computed h_{FE} values. In this case the base is, of necessity, formed by ion implantation as can be seen from Fig. 2(c).

Fig. 3 gives curves of f_t and f_{mosc} for the three transistors as a function of collector current I_c. These curves are taken directly from the BIPOLE output (see Table, Appendix 3 for the SP2A3 device). It is emphasised here that these were considered the most important output parameters (for a given collector doping and breakdown voltage) and it was the corresponding tables of f_t and f_{mosc} that were scanned for each manual iteration on the profile parameters, the goal being to achieve maximum f_{mosc} over a maximum range of d.c. collector current, while maintaining a value of h_{FE} greater than or

equal to f_t/f_s over the current range. For this manual 'optimization' process we used the data from the analytic output discussed in section 2.1, to choose the value of stripe width L, collector doping level, N_{epi}, and collector epitaxial layer thickness X_{epi}. Fine adjustment of X_{epi} was made using the BIPOLE program once the impurity profile had been determined, (thus fixing the junction depths X_{j1}, X_{j2}). The value of X_{epi} was reduced until the value of breakdown voltage V_{cbr} (computed using the ionization integral in plane coordinates in BIPOLE) started to decrease. This results in a design in which the collector epitaxial layer is slightly in reach-through at high voltages. In studying the 915 MHz device, we also examined the performance for a planar device using the ionization integral in cylindrical coordinates, suitably reducing the epitaxial layer thickness. It is important to note the importance of this part of the design. Too high a value of X_{epi} will increase the value of the collector series resistance, thus increasing not only the static V_{cesat} but also the high frequency capacitive current loss through the C_{jcb}-R_c network; this results in a double source of power conversion efficiency degradation. Too low a value on the other hand, will decrease V_{cbr}.

It should be noted that the use of the ionization integral in plane co-ordinates for the calculation of V_{cbr} implies the use of a structure in which mesa, moat-etch or similar [18] fabrication techniques are employed to yield maximum possible V_{cbr} values.

When the manual iteration process described above has given an apparently 'optimum' structure, the BIPOLE program is run a final time to generate the corresponding model parameters or tables, which are directly stored on a disc to be accessed by the WATAND program.

3. Model Generation and Evaluation

3.1 Types of Model Used

The most widely used CAD model of the bipolar transistor is undoubtedly that of Ebers-Moll. In its 'extended' version [11], including junction and diffusion capacitance, base resistance, gain (h_{FE}) variation with current, it is capable of predicting static and dynamic performance up to the current determined by the onset of high level effects - mainly Kirk effect. BIPOLE generates the extended Ebers-Moll model parameters and they are stored directly on a disc for access by WATAND.

In the course of this project it was observed that significant high frequency power loss can occur in the collector resistance due to the capacitive current through C_{jcb} (see Appendix 1.3). The model finally adopted is shown in Fig. 4(a). The maximum collector current and voltage for which it is valid are printed in the file title and in its subsequent use in the class C or E circuit study, it is most important that these values not be exceeded.

The Gummel-Poon model parameters may also be generated by BIPOLE. This model gives fair accuracy in predicting high level effects (h_{FE} and f_t fall-off). The modified version (with R_c and C_{jcb} divided into sections as used in this project) is shown in Fig. 4(b).

The multi-sectional tabular model [15, 16], developed by the authors of this report specifically for use with BIPOLE and WATAND, has also been used in this project. The model consists of an array of values of emitter and collector currents and charges tabulated for selected values of V_{be}, and V_{bc}. Non-linear collector and base resistance are also tabulated. This piecewise linear model has the advantage of taking all known high level effects into account without any analytic approximations, the additional non-linear behaviour being implicitly described by the numerical solutions of the carrier transport equations within BIPOLE. This model (Fig.4(c)) can be split into any desired number of lateral sections but because of execution time limitations, only one main section plus a peripheral section were used in this project. The collector resistance is normally modeled as a function of both I_c and V_{cb}. However for this project, it is modeled only as a function of V_{cb} (thus being more accurate at high frequencies where the saturation voltage is not reduced by conductivity modulation of the collector epitaxial layer).

3.2 Comparison of the Three Models

Results obtained using each of the three models in a Class C circuit are shown in Fig. 5. The results are seen to be in close agreement with each other. Note however, that operation has been restricted to currents less than or equal to the Kirk current I_k. Beyond this value, the Ebers-Moll model is invalid. Since we did not seek to determine precise maximum power handling capabilities of the transistors used in this study, this is not a limitation. If the study were to be pursued further to determine critically the maximum power output, then either the Gummel-Poon or BIPOLE tabular models would have to be used.

3.3 Parametric Effects

To test for the parametric effects of the transistor model on the performance of the circuit simulation, the Ebers-Moll model was chosen and the nonlinear collector junction capacitance C_{jc} was replaced by a constant 'average' capacitance, $(=(1/7)C_{jc}$ evaluated at $V_{cb} = 0)$. One point of η vs. G_p was generated at one conduction angle. The result is included in Fig. 5. It can be seen that by using the constant capacitance, a more optimistic result is obtained. In fact, the result will depend on the value of the 'average' value chosen for the junction capacitance. This study indicated that the proper modeling of the nonlinear capacitance in the transistor is advisable for obtaining realistic results, especially in class C and class E power amplifier applications.

3.4 Experimental Verification

The 2.45 GHz class C amplifier analysed in this project uses a Silicon transistor (SP2S2) with a peak f_t of 6.1 GHz and f_{mosc} of 19GHz, or for the GaAs case (SP2A2) a peak f_t of 10.7 GHz and a similar f_{mosc}. For experimental verification of the models in a similar environment, we chose a low frequency power transistor whose f_t is approximately 10 MHz at the current used and whose value of f_{mosc} is about 76 MHz. The basic details of this transistor (LFP) are listed in Table 1. It may therefore be considered a crudely scaled version of the real microwave transistor and circuit. The impurity profile and mask data, were used as input to the BIPOLE program to generate the extended Ebers-Moll model for use in the WATAND simulation.

In order to examine the non-linear behaviour, the circuit shown in Fig. 6 was used. Fig. 7 shows computed and measured efficiencies as the tank circuit capacitance is varied above and below resonance. The aggreement between computed efficiencies using the BIPOLE-WATAND system and the measured efficiencies is evident from the Figure. Five values of input voltage V_s were used. The experimental accuracy of setting V_s was not better than 5%. The difference between measured and computed maximum efficiency is -4%, +2%, -4% for V_s 13.5, 15, 16.5 respectively. However, of particular significance in the results of Fig. 7 is the fact that as the input V_s is increased above the value corresponding (visually, on the oscilloscope) to the onset of saturation, the efficiency rises somewhat (to 91%) and then starts to decrease. On the WATAND simulation, the same general behaviour occurs, with the efficiency peaking at 87%. It should be noted that this error could be due not only to the computer modeling but also to experimental errors and to differences between the measured impurity profile (supplied by the manufacturer) and the actual profile. The weakest link in the model verification at the time of writing is in the collector resistance. The experimental results are in the process of being extended to higher collector currents and voltages to check this point.

4. Class-C Circuit Design and Results

4.1 Preliminaries

The objective of a power amplifier design is to select a device and a circuit configuration which give at a given frequency, maximum efficiency for a given power gain (or maximum power gain for a given efficiency). What is meant by efficiency and power gain, will be explained below. Class-C amplifiers have long been used as power amplifiers [3], where electronic tubes are used in the basic design. With the advent of solid-state technology, transistors became the basic devices used in circuit designs. Almost all the published work on Class-C transistor amplifier design use analytic approaches which employ approximate transistor models, in order to obtain some meaningful results [3-10]. These methods and models, however, become inadequate when the the transistor operates at very high frequencies such as in microwave applications. At these high frequencies a more complicated model is needed and advanced numerical and computer simulation techniques become a necessity.

The theory of Class-C amplifiers can be found in many textbooks (see for example, [12]). The basic quantities and variables that define the operation of a Class-C amplifier are given in the following. These quantities are interrelated and interdependent.

1) Supply Voltage V_{cc}: determined by the transistor breakdown voltage. The maximum supply voltage should be less or equal to one half the rated breakdown voltage.
2) Conduction Angle: is determined by the input bias and the input signal.
3) Maximum Collector Current: determined by the transistor design.
4) Load Resistance: Once the bias is set, the load resistance, R_L, is chosen to cause the transistor to operate at the verge of saturation.
5) Output Power: $P_{out} = V^2/(2R_L)$, where V is the amplitude of the fundamental component of the voltage waveform across R. (Note that for a given V, the lower R_L is the higher P_{out} will be. However low R_L will produce high collector current. Thus for a fixed supply voltage, the output power is limited by the maximum collector current).
6) DC Power: $P_{dc} = V_{cc} I_{dc}$ where V_{cc} is the supply voltage and I_{dc} is the dc component fo the voltage waveform passing through V_{cc}.

7) Input Power: $P_{in} = V_{in} I_{in}^{*}/2$, where V_{in} and I_{in} are the phasor representations of the fundamental components of the voltage and current waveforms at the input part to the transistor. Alternatively, P_{in} can be measured as the power available from the input generator when the generator is matched to the transistor input port.

8) Efficiency $\eta = P_{out}/P_{dc}$

9) Power Gain $G_p = P_{out}/P_{in}$

A basic Class-C amplifier circuit is given in Fig. 8.

4.2 Computer-Aided Circuit Design

For computer-aided circuit design to be practical and efficient, three basic requirements should be available: (1) fairly accurate device modeling technique, (2) fast and relatively accurate circuit analysis program, and (3) easy use of computer programs, such as interactive computing facilities. A fourth requirement which is also useful and sometimes necessary is the availability of optimization, sensitivity and tolerance routines. We should stress here that the human designer is an indispensable part of our design loop.

Here at the University of Waterloo, all the above requirements and facilities are available. First, a computer program called BIPOLE, which has been described in the previous section, is available for generating numerical models of bipolar transistor from device fabrication data. Secondly, in order to analyze Class-C amplifier circuits, a non-linear transient analysis program is needed to simulate the circuits efficiently. In addition, a steady-state algorithm as well as a Fourier analysis subroutine are required. All these routines are part of WATAND, which has been developed here at the University of Waterloo. Optimization and sensitivity routines have not been used in the present study. The third requirement, which is essential to this study is the implementation of WATAND in an interactive mode on an IBM 370/158 using CMS/VM. This facility allows the problem data to be typed at a terminal and the results of the analysis displayed on a screen. Any changes in the problem parameters can be done interactively and updated results can be obtained almost instantaneously. A WATAND file for the circuit given in Fig. 8(a) is shown in Fig. 8(b).

The steps followed in the Class-C circuit design process are as follows: (see Fig. 9 for a flow chart of the procedure).

(1) Get numerical model of the transistor (extended Ebers-Moll) from BIPOLE. This includes maximum collector current I_K (Kirk effect) and collector breakdown voltage.

(2) Set supply voltage less than or equal to one half the breakdown voltage.

(3) Select an output tank circuit tuned at the desired frequency.

(4) Set the input bias for a given conduction angle. At this stage an input matching circuit is not used.

(5) Set the input signal and choose a load resistance R_L so that the collector current does not exceed the maximum value specified by the model and such that the transistor is on the verge of saturation. This step may involve many iterations which include retuning the output circuit and adjusting the input source. The interactive facility is found to be indispensable during this step. The steady-state algorithm is also a necessity, otherwise the transient analysis becomes prohibitively expensive [17]. We shall refer to the case where the transistor touches but does not enter into saturation as the non-saturated Class-C amplifier design, see Fig. 10. By carrying out sensitivity studies, however, we have discovered that by driving the transistor slightly into saturation, improvement in both efficiency and power gain was obtained. We shall refer to this case as the saturated Class-C amplifier design (see Fig. 11).

(6) Compute the Fourier coefficients of the input current and voltage waveforms, output voltage and the current through the dc supply.

(7) Use the results of step 6 to compute the input power at the fundamental, output power and dc power; then compute the efficiency and the power gain.

(8) In order to obtain a different set of values for the efficiency and the gain, change the conduction angle by changing the input bias and then go to step 5. In this way a relation between the efficiency and the power gain for a particular transistor is obtained (see Fig. 12). If the results are not satisfactory, the transistor fabrication data are altered in the input data to BIPOLE and the computer aided analysis is restarted from Step 1.

4.3 Input Matching and Stability

In practice, an input matching circuit is designed to match the input impedance of the transistor to the impedance of the generator. In addition an input tuning circuit may be employed. The power input is then calculated as the power available from the generator. However, when an input tuning is used, the circuit may become unstable. This instability is caused by the feedback from the output to the input through the collector-base capacitance. Thus in designing the input circuit, extreme care should be taken so as not to cause the circuit to become unstable. One way of checking for stability of the circuit on the computer is to obtain a linearized model of the circuit and then compute the poles and zeros of the transfer function between the input and the output. Such a program called ANP3 (which has been developed at the Technical University in Denmark) is available on our system here at the University of Waterloo.

4.4 Common-Base vs Common-Emitter Configuration

We have tried both common-emitter and common-base configurations in our Class-C circuit design. We have found that the common-base configuration has better stability properties than the common-emitter configuration. This may be due to the fact that since the transistor is cut-off during most of the cycle in a Class-C operation, the common-base configuration tends to disconnect the output from the input, while in the common-emitter configuration the collector-base capacitance connects the output to the input for most of the cycle which creates the instability problem due to the feedback.

In a previous report [1], we have investigated the problem of input matching and stability and showed that with the proper matching between the input source and the transistor, the performance of the amplifier (η vs. G_p) will approach the performance of the amplifier assuming ideal matching (i.e., input source has very low series resistance). Thus in this report we assume ideal matching and consider the common-emitter configuration since there are no stability problems.

4.5 Discussion of the Results of Class-C Circuit Design

A large number of transistor designs and circuit configurations have been investigated. We give here a summary of the results which in our opinion are most useful and feasible. These results represent a small fraction of the total cases studied in this project.

Different transistors were designed and studied at two different operating frequencies. The performance of one transistor, SP9S1, has been studied at 914 MHz and the results reported in a previous report [1] and also in this report in the section on transistor model comparison.

In this report we limit the detailed discussion to the performance of transistors designed to operate at 2.45 GHz. We present the results of the performance of two such transistors. One is a Silicon transistor, SP2S2E, and the other is a Gallium-Arsenide transistor, SP2A2E. (Note: the 'E' refers to the Ebers-Moll Model).

4.5.1 Silicon Transistor (SP2S2E) Results at T = 27°C

The performance of the transistor in a Class-C amplifier circuit was evaluated with WATAND using the BIPOLE generated extended Ebers-Moll model. Initially, the Class-C amplifier was designed to touch saturation, but not enter into it. This design is referred to as the "non-saturated" case. After carrying out sensitivity analysis, however, we discovered that by driving the transistor slightly into saturation, we could obtain improvements in the $\eta - G_p$ curve. This design, where the transistor is driven slightly into saturation, is referred to as the "saturated" case. The $\eta - G_p$ curves of both the non-saturated and the saturated cases as well as that of SP2S2E in a Class-E amplifier circuit configuration, are all shown together on the same figure (Fig. 12). Note that the power output in the Class-C amplifier circuit configuration is about 22 watts and in the Class-E configuration is about 18 watts. Note also that the performance of SP2S2E in the saturated Class-C amplifier circuit configuration is better than its performance in a Class-E configuration at this power output level.

Fig. 13 shows the $\eta - G_p$ curves of SP2S2E in saturated Class-C and Class-E configurations at a lower power output level of about 11 watts. Note

that for low power gain ($\leq$ 13) the performance of the transistor in the Class-C configuration is better than its performance in the Class-E configuration, and vice versa when $G_p > 13$.

4.5.2 Gallium Arsenide Transistor (SP2A2E) Results (Class C) at T = 27°C

The transistor described in our previous report [2] using Gallium Arsenide, SP2A2E, was evaluated with WATAND using the BIPOLE generated extended Ebers-Moll Model. The results at 2.45 GHz are shown in Fig. 14, together with the results using the Si transistor SP2S2E. In both cases the transistors operate in non-saturated Class-C amplifier circuits. The improvement in efficiency is probably due mainly to the reduction in the collector resistance (due to the higher electron mobility), (0.024 ohm for GaAs compared to 0.156 ohm for S_i for the total active area of 1.5 µm x 1.33 cm.)

4.6 Sensitivity Analysis of SP2S2E in a Class-C Circuit

To study the effects of small changes in circuit parameters on the performance of SP2S2E in the Class-C amplifier deisgn, a point is selected on the $\eta - G_p$ curve of Fig. 13, at η = 92.3%, G_p = 7.32 and P_{out} = 10.7 watts. Notice however that sensitivity analysis is, in fact, carried out when generating each point on the $\eta - G_p$ curve. The results of the sensitivity analysis for the selected point are shown in Fig. 15. Note that almost all the points lie below the original $\eta - G_p$ curve. However, we can see that if R_L is increased, the performance will improve. This does not mean that by increasing R_L the whole $\eta - G_p$ curve will improve, rather the sensitivity analysis indicates that by increasing R_L the performance at that particular point will improve.

5. Class-E Circuit Design and Results

Published studies of Class E operation of tuned power amplifier [19,20] assume idealised operation. In our work reported here we study their operation at microwave frequencies 915 MHz and 2.45 GHz, using numerical techniques in which the true behaviour of the transistor under design has been modeled as accurately as possible. These modeling techniques have been described in earlier sections. For our Class E studies we restricted the models to the extended Ebers-Moll models of the Silicon transistor: designated SP9S1E (for 915 MHz) and SP2S2E (for 2.45 GHz), and discussed in section 3.

All of our Class E studies were carried out at one temperature only (27^{o}C), and we discuss here only the 2.45 GHz case. Our results for SP9S1E were given in [2].

We studied only the common emitter Class E configuration, as shown in Fig. 16A ; in Fig. 16B , we show the WATAND file describing this circuit for one particular set of element values (in fact those corresponding to point 4 of Fig. 13).

Application of the Sokal/Raab idealized design for maximum efficiency [19, 20] yields the following results:

Since the maximum peak voltage v_{ce} allowed for transistor SP2S2 is 31.7 volts,then V. CC = 31.7/3.56 = 8.9 V.

Since our maximum peak collector current for the transistor is 8.8 A, then the dc current I for the source V. CC should be 8.8/2.84 = 3.1 A. Hence, the idealised input dc power is 3.1 x 8.9 = 27.5 W. Since for idealised design we obtain 100% efficiency, this yields idealised output microwave power = 27.5 W. The resistive dc load presented by the amplifier to the dc power supply is R_{dc} = 8.9/3.1 = 2.9 Ω. Hence the optimum load resistor R.L = R_{dc}/1.734 = 1.67 Ω. Using Raab's design equations for an assumed output-circuit Q of 7 yields the following:

$$L_2 = (R.L * Q)/\omega = 0.76 \text{ nH};$$

from $(\omega^2 L_2 C_2 - 1)/\omega C_2 = 1.15$ R.L we obtain C_2 = 6.6 pF;

from $\omega C_1 = 1/(1.545$ R.L) we obtain C_1 = 7 pF.

L_1 is to be chosen large enough to yield an approximation to a constant current source.

According to Raab, for idealized switching action of the transistor with a 50% duty cycle, this should yiled a microwave sinusoidal voltage across R.L of amplitude 9.56 V, and a 100% efficiency operation with output power of 27.5 watts.

Because we cannot expect such idealized operation at 2.45 GHz, these design values are not achievable.

As discussed in [1] we proceeded to an achievable design by making successive manual iterations combined with trial and error tuning techniques, using the WATAND simulator. In this way we obtained two "maximum efficiency designs": the first is a "low power design" yielding an output power of 12.3 watts at a power gain of 4.7 and an efficiency of 92.8%; the second is a "high power design" yeilding an output power of 18.5 watts at a power gain of 8.9 and an efficiency of 87.1%. The element values and corresponding performance Figures are shown in Table 2, together with those for the Raab optimum design previously discussed.

Starting from these two designs, we used sequences of changes of source voltages (together with minor tuning adjustments of component values) to yield points of lower efficiency but higher microwave power gain. The results are shown in Table 3A for the low power design and in Table 3B for the high power design. Plots of η versus G_p are shown, with the corresponding saturated and unsaturated Class C configuration curves, in Figs. 13 and 12 respectively.

Results of some sensitivity tests run on two of the (low power) Class-E points (points 4 and 8 of Table 3A and of Fig. 13) are given in Figs. 17 and 18. It will be noticed that the effect of a small variation in any one of the circuit parameters is to move the point in $\eta - G_p$ plane approximately parallel to the original Class-E plot. This indicates that the Class-E points shown in Fig. 13 are approximately at some local optimum for Class-E operation.

Waveforms of v_{ce} and i_c (into the active part of the transistor) for the same two points [4 and 8] are shown in Figs 19, 20.

6. Effects of Temperature and Parasitics for Class-C Circuit

6.1 Performance at Higher Temperatures

The new temperature subroutine in BIPOLE takes account of mobility and saturated drift velocity variation in an empirical manner. The Fortran expressions used are given in [2] together with diagrams of computed mobility - doping level - temperature curves superimposed on data from the literature [22] for both S_i and GaAs [21, 23].

WATAND simulated results using BIPOLE generated Ebers-Moll Models for 27°C, 100°C, 150°C, 200°C are shown in Fig. 21 for the Silicon and in Fig. 22 for the Gallium Arsenide Class C amplifiers at 2.45 GHz. In all cases the transistors operate in non-saturated Class-C amplifier circuits. It is seen that the efficiency decreases initially (as the temperature rises) but stops decreasing and even increases in certain regions at higher temperatures. The BIPOLE generated values of collector resistance are shown for each temperature, since this is one of the major sources of inefficiency.

6.2 Effects of Parasitics on SP2S2E

The effects of major parasitics on the performance of SP2S2E in a saturated common-emitter Class-C circuit configuration has been investigated. These parasitics are the emitter ballast resistance R.E, emitter inductance L.E and collector-to-base and emitter-to-base bonding pad capacitances. The effects of each of these parasitics on the performance of the transistor were investigated separately; i.e., when one parasitic is present and the other two are not. Various values of these parasitics were considered. The results are shown in Fig. 23.

As stated in [2], a suitable value of emitter ballast resistance can be estimated crudely by reasoning that at the maximum collector current (8 A for the SP2S2) the ballast resistance R.E must maintain the current in each emitter finger at approximately the same value even if the temperature varies over the chip. Using $\Delta V = I \times R.E = 0.2$ V gives R.E $\simeq$ 0.02 ohm. This is, of course, split up and distributed in series with each emitter finger.

Note that the parasitics may have a drastic effect on the performance of the transistor and effort should be spent in the fabrication process to reduce these parasitics as much as possible. Generating curves as those given in Fig. 23, would help to determine the level of parasitics tolerable to an acceptable performance. For example, the bonding pad capacitance is determined by the area of the metalization and the oxide thickness. Since the area will be determined by the current and by practical bonding considerations, this capacitance can be reduced by growing a thicker oxide.

7. Preliminary Study of Microwave Rectifier Diodes

7.1 Diode Design

For a simple N-P junction, whether diffused or double epitaxial, the response time is limited by the diffusion transit time across the lightly doped region to $t_b = w_b^2/2D_n$. For a 1 micron base width corresponding to a maximum breakdown voltage of 28 V for S_i (30 V for GaAs), the corresponding frequency ($1/2\pi\ t_b$) is 950 MHz for Si (5.7 GHz for GaAs). The only reasonable solution therefore appears to be Schottky barrier diodes.

The two significant quantities for Schottky barrier rectifiers are the depletion layer capacitance and the series resistance. On Fig. 24, we have listed the salient parameters for a set of such diodes using Silicon and GaAs. The optimum area is not immediately evident. Too large an area will clearly reduce the power conversion efficiency due to the diode capacitance and circuit resistance. Too small an area on the other hand, will also reduce the efficiency because of the non-negligible diode series resistance. We have therefore selected two areas for each diode (a low voltage (34 V) for use at the edge of the rectenna and a higher voltage (110 V) for use at the centre of the rectenna).

7.2 Diode Evaluation

Since this is purely a preliminary study, we selected after trying several circuit configurations, the simple circuit shown in Fig. 24, for the WATAND analysis. The generator is assumed to be a half wave dipole. To simulate a situation close to a possible real rectifier circuit, we have included one shunt inductor (so that all the d.c. power is being dissipated in the load) and one smoothing capacitor across the load. The maximum obtainable efficiency with this circuit was computed on WATAND to be 78.6% using an ideal, lossless diode with zero capacitance. The actual efficiency, (defined as the ratio of d.c. power in the load to available r.f. power from the 72 Ω generator) is listed in Fig. 24. This maximum was found to occur when the inductance was "resonated" with the average diode capacitance. The value of L was found in each case with successive manual iterations within the WATAND

environment on CMS.

From these results it is seen that the 34 V diode comes within 1% of the efficiency of an ideal diode and the 110 V diode is about 4% lower than that of an ideal diode at 2.45 GHz, using GaAs.

A complete study would require modeling the antenna at d.c., the fundamental and the next few harmonics with a more complex filtering circuit.

8. Conclusions

In the course of this study we have demonstrated that it is technically possible to achieve 80% efficiencies with 10 dB of power gain at 2.45 GHz, using currently available silicon technology. The use of GaAs improves the performance over the range of interest at 27°C and shows distinct advantages in terms of efficiency for a given power gain at higher operating temperatures, i.e. close to those which will probably be encountered in the space environment.

The choice of class C versus class E is not clear cut. However, it would appear (using the modeling and simulation techniques described in this report) that there is no significant advantage to be gained by using class E compared to slightly overdriven (i.e. slightly saturated) class C operation. The results of the class C versus class E comparison are clear from the Figures. It must be noted that in drawing any practical conclusions, the class E circuit is, at least in its low frequency form, distinctly more complex. This complexity (apart from the extra high inductance required) manifested itself in the computer aided design of a circuit to give the best 'efficiency-power gain' combination.

With reference to the fabrication details of the transistors, the following remarks should be noted. To obtain collector-base breakdown voltages near to the maximum value limited by 'plane' bulk breakdown, p^- moat or moat etch process has been assumed throughout. The effect of using planar technology was discussed in our first report [1] and although the performance was worse, the degradation was perhaps not as bad as could be expected, after re-adjusting the epitaxial layer thickness. In the case of the silicon design, an arsenic diffused emitter is assumed throughout; this virtually eliminates emitter dip effect and gives a sharply decreasing profile in the vicinity of the emitter-base junction, which is favourable in reducing excess charge in the emitter, and thus maintaining high f_t values. In the case of the GaAs design, we have not yet found complete data in the literature, specifically on band-gap reduction effects at high emitter doping levels. However, the microwave characteristics are determined essentially by the base and collector regions. If the emitter proved to be a problem, either because of reduced emitter injection efficiency (too small a value of h_{FE}) or because of too high an excess minority

carrier charge concentration, then presumably use of a heterojunction structure using GaAlAs, could overcome this problem. We stress again the importance of choosing the epitaxial layer parameters carefully in order to obtain the computed values of efficiency. This requires careful control of the fabrication process to minimize, or to compensate for, out-diffusion of donor atoms from the heavy doped substrate. With epitaxial layers of the order of 2 μm thick (after processing), this is clearly important. We stress also that all of our proposed designs necessitate ion implantation of the base. Since the active base region conductivity is one of the most important parameters, any transistor made by standard double diffusion methods would necessarily perform less well (see also [1]).

The final design presented in Appendix 3, is a slightly modified version, SP2A3, of the SP2A2 transistor, in which we have simulated diffused (or implanted) shallow layers on both the emitter and base near the surface. The goal here was to reduce the extrinsic component of base resistance which was limiting the performance in the SP2A2 GaAs design. The improvement from 19 to 32 GHz in the maximum oscillation frequency is quite significant. An alternative approach would be simply to introduce an N_A^+ layer in the extrinsic base region.

Finally let us recall that although the low frequency experimental comparison appears to substantiate the BIPOLE-WATAND modeling technique used, an obvious next step would be a microwave experimental power converter. In order to be meaningful, this should be performed with a transistor whose fabrication data, (impurity profile, carrier lifetimes, etc.) are accurately known. It need not, at this stage of the project, be a structure optimised for the SPS design, but would simply be used to verify some of the basic features of the problems specifically related to microwave packaging, parasitics, etc.

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	Units	SP9S1	SP2S2	SP2A2	LFP
B	cm	1.0	1.33	1.33	2.46
L	μm	2.0	1.5	1.5	260
X_{epi}	μm	3.5	2.0	2.00	80
N_{epi}	cm^{-3}	8×10^{15}	2.5×10^{16}	2.5×10^{16}	0.9×10^{14}
X_{j1}	μm	0.3	0.20	0.147	7.5
X_{j2}	μm	0.6	0.37	0.429	19.0
ρ_{e_e}/sq	ohm	22	31	93.9	0.44
ρ_{e_b}/sq	ohm	311	447	1520	75.5
$\rho_{e_{be}}/sq$	ohm	2640	3530	2170*	419.0
V_{cbr}	V	62.7	31.7	33.	1340
V_{ebr}	V	6.3	6.5	--	12.8
I_K	A	2.8	8.8	8.8	10.1
X_{jbim}	μm	0.4	0.22	0.22	-
N_{jbim}	cm^{-3}	1×10^{18}	2.0×10^{18}	2×10^{18}	-
X_{bim}	μm	0.07	0.05	0.10	-
$f_{t\ max}$	GHz	2.89	6.14	10.7	0.016
f_{mosc}	GHz max	19.1	19.9	19.4*	0.110
W_{nom}	watts	22.	35.	36.	1690.

Table 1. Summary specification and performance data of three sample transistors studied in the course of this project.

Note: For the implanted profiles $X_{bim} = \sqrt{2}\,\sigma$,

$$N_{jbim} = \phi/(\sqrt{2\pi}\,\sigma)$$

$$X_{bim} = x_p$$

$$n(x) = [\phi/\sqrt{2\pi}\,\sigma]\ \exp-[(x - x_p)/\sqrt{2}\,\sigma\ ]^2$$

* see section 8.

	V.CC (V)	V_{ce} Peak (V)	i_c Peak (A)	dc Power (W)	Micro-wave Power out (W)	η %	c Micro-wave Ampli-tude (V)	R.L Ω	L.2 nH	C.2 pF	C.1 pF
Raab (ideal)	8.9	31.7	8.8	27.5	27.5	100	9.56	1.67	.76	6.6	7
Design 1	9.8	31.4	5.3	13.7	12.3	92.8	5.9	1.4	.7	8.5	0*
Design 2	10.0	27.9	8.5	21.3	18.5	87.1	5.4	.8	.365	17	9*

*Note: It must be remembered that the transistor itself presents a collector to emitter capacitance of the order of 5pF to 10pF.

Table 2: Class E Designs.

#	R.S (Ω)	R.L (Ω)	V.CC (V)	V.BB (V)	V.S (V)	C.1 (pF)	C.2 (pF)	L.2 (nH)	L.1 (nH)	η (eff.)	Gp (abs.)	Po (Watts)	V peak (V)	I peak (A)
1	.25	1.4	9.8	.5	2.7	0	8.5	.7	8.7	92.8	4.7	12.3	31.4	-
2	.25	1.4	9.8	.5	2.6	0	8.5	.7	8.7	92.4	5.2	12.1	31.0	-
3	.25	1.4	10.0	.5	2.6	0	8.5	.7	8.7	91.1	6.7	12.1	31.1	-
4	.25	1.4	9.8	.52	2.1	0	8.6	.71	8.7	90.5	7.3	9.8	29.3	4.6
5	.25	1.4	9.8	.5	2.0	0	8.5	.71	8.7	89.0	9.2	9.9	29.1	-
6	.25	1.4	9.8	.6	1.8	0	8.6	.7	7.8	87.2	13.0	10.2	29.2	-
7	.25	1.4	9.8	.6	1.6	0	8.6	.7	7.8	83.7	18.8	9.5	28.5	-
8	.25	1.4	10.7	.6	1.6	0	8.6	.7	7.8	80.4	27.6	11.3	31.4	4.8
9	.25	1.4	10.8	.6	1.5	0	8.6	.7	7.8	76.6	34.7	10.7	30.9	-
10	.25	1.4	10.8	.6	1.4	0	8.6	.7	7.8	72.0	39.6	9.6	29.7	-

Table 3A: Parameter Values and Results for Class-E at Low Power (shown plotted in Fig. 13)

#	R.S Ω	R.L Ω	V.CC V	V.BB V	V.S V	C.1 pF	C.2 pF	L.2 nH	L.1 nH	η	Gp abs	Po W	V peak V	I peak A
1	.25	.8	10	.5	2.7	9	17	.365	4.35	87.1	8.1	18.5	27.9	8.5
2	.25	.8	10	.5	2.6	9	17	.365	4.35	86.5	8.9	18.2	27.7	8.4
3	.25	.7	10	.5	2.7	9	17	.365	4.35	87.2	8.0	17.7	28.7	8.73
4	.25	.7	10	.5	2.7	8	17	.365	4.35	86.1	8.6	18.3	29.6	8.94
5	.25	.7	10	.5	2.5	9	17	.365	4.35	85.8	9.7	17.3	28.4	8.6
6	.25	.7	10	.7	2.5	9	17	.365	4.35	70.3	24.4	13.2	25	6.1
7	.25	.7	10	.75	2.5	9	17	.365	4.35	71.1	24.9	14.1	26	7
8	.25	.7	10	.8	2.5	9	17	.365	4.35	72.7	25.0	14.8	26.5	7.5
9	.25	.7	10	.85	2.5	9	17	.365	4.35	74.1	24.9	15.3	26.9	7.8
10	.25	.7	10	.95	2.5	9	17	.365	4.35	75.4	24.7	16.2	27.5	8.3
11	.25	.7	10	1	2.5	9	17	.365	4.35	74.9	24.8	16.6	27.7	8.4
12	.25	.8	10	.95	2.5	9	17	.365	4.35	75.4	24.6	16.7	26.6	7.9
13	.25	.9	10	.95	2.5	9	17	.365	4.35	75.3	24.1	17.0	25.8	7.8
14	.25	.9	10	1	2.5	9	17	.365	4.35	75.2	24.9	17.6	26.1	7.9
15	.25	.9	10	1	2.3	9.5	17	.365	4.35	75.2	24.5	17.5	25.8	7.8
16	.25	.9	10	1	2.5	9.5	17	.362	4.35	74.5	24.9	17.8	25.7	7.9

Table 3B: Parameter Values and Results for
Class-E at High Power (shown plotted in Fig. 12)

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Maximum frequency of oscillation

The maximum frequency of oscillation of a bipolar transistor is given by:

$$f_{max\ osc} = \sqrt{f_t / (8\pi r'_{bb} C_{jc})} \quad (1)$$

This assumes that the transistor is loaded at its output by a resistance equal to its output resistance at high frequencies

$$R_L = r_{out} = (C_n / C_{jc}) / g_m \quad (2)$$

The value of f_t expressed in terms of the device physical parameters, neglecting emitter neutral region charge, collector R-C time constant, and the low current $r_e(C_{je} + C_{jc})$ term, is simply:*

$$(1/2\pi f_t) = t_{bb} + t_{bc} \quad (3)$$

$$= w_b^2 / 2D_n + w_{sc} / 2v_{sat} \quad (4)$$

The base resistance is related to the physical parameters by:

$$r'_{bb} = L / (12 w_b \sigma_b B) \quad (5)$$

and the collector-base transition capacitance is given by:

$$C_{jc} = \varepsilon L B / w_{sc} \quad (6)$$

The expression for $f_{max\ osc}$ thus becomes:

$$f_{max\ osc} = \frac{1}{L} \sqrt{\frac{12 \sigma_b w_b w_{sc}}{8\pi\varepsilon (w_b^2/D_n + w_{sc}/v_{sat})}} \quad (7)$$

It is clear that this quantity may be optimized in terms of the relative values of w_b and w_{sc}. Differentiating w.r.t. w_b and setting the result equal to zero gives the required condition:

$$w_b^2 / D_n = w_{sc} / v_{sat} \quad (8)$$

The final value of optimized f_{mosc} is therefore:

$$f_{max\ osc\ opt} = (1/L) \sqrt{(3 v_{sat} / 4\pi^2 \varepsilon)(D_n / v_{sat})^{1/2} \sigma_b w_{sc}^{1/2}} \quad (9)$$

* The expression for t_{bb} can incorporate any 'drift field factor' in the actual numerical value used for D_n.

From the high frequency equivalent circuit it is a simple matter to show that the output resistance r_{out} of the common emitter stage is:

$$r_{out} = [(\omega_t/2)C_{jc}]^{-1} \qquad (1)$$

where C_π is the total capacitance at the input node of the hybrid-π equivalent circuit due to excess charge in the neutral base, neutral emitter and in the collector-base s.c.l.

$$C_\pi = g_m t_{ec} + (I/v_t) t_{et} \qquad (2)$$

where $t_{et} = t_{bb} + t_{scl} + t_e$ (3)

$$t_{bb} = W_{bo}^2/2D_n \qquad (4)$$

$$t_{scl} = w_{scl}/2v_s \qquad (5)$$

and $C_{jc} = (\varepsilon A_c/W_{scl}) F_{cjc}$ (6)

we thus obtain:

$$r_{out} = [\varepsilon E_{bn}^2 / 4q^2 \nu_s] (F_{escs}/F_{cjc})(1/BL)(1/N_{dc}^2) \qquad (7)$$

Note that the factor F_{cjc} (≥ 1) allows for the fact that the base-collector junction surface is larger than the emitter surface and the factor $F_{escs} = 1 + (t_{bb} + t_e)/t_{scl}$ is close to 2 in a transistor optimized for maximum high frequency gain (maximum $f_{max\ osc}$).

Load resistance for maximum class A power output

To obtain maximum class A output power the load resistance R_L must be chosen such that:

$$R_L = V_{ctr}/I_{cmax} \qquad (8)$$

where V_{ctr} is the collector-base breakdown voltage (for low impedance inputs, this is approximately the same as the collector-emitter breakdown voltage):

$$V_{ctr} = V_{...} + \frac{q N_{dc}}{2\varepsilon} (W_{scl} - x_{...})^2 \quad \text{where } F_{...} < 1/(4\pi \omega_t \tau_{...}) \qquad (9)$$

and I_{cmax} is the maximum value of collector current. For most circuits this can be considered to be the current at which base widening (Kirk effect) just starts to occur:

$$I_{cmax} = A_{...} q N_{dc} v_s \qquad (10)$$

where

$$A_{emax} \geq (\pi \cdot ...)(W_{...}) \qquad (11)$$

here, $W_{...}$ is the "punch through" width of the epitaxial layer.

Combining (8) and (9) gives:

$$R_L = [\varepsilon E_{bn}^2 / 2q^2 \nu_s] (F_{wcbr}/F_{c\,max})(1/BL)(1/N_{dc}^2) \qquad (12)$$

Combining (7) and (12) gives the ratio of R_L/r_{out}:

$$R_L/r_{out} = 2 F_{...}(F_{...}/F_{...}) \approx F_{...}/2 \qquad (13)$$

Since $F_{...}$ is a geometrical factor, a typical value of which is 2 for microwave devices, we see that the resistance for maximum power output is nearly equal to the resistance for maximum low frequency gain. In other words, optimal output matching should yield nearly the maximum power [illegible] from the transistor.

Appendix 1.3:Outline of the analytic approach used

Here, we summarize the method used to derive initial data to be used as input to the BIPOLE program and to generate the curves shown in Fig.1. Reference [6] was used extensively to rough-out the design by calculating the gain and 'current limited' efficiency η_I (ETAI in the computer output example of Appendix 2). Equation (15) of [6] gives:

$$AI^5 = I_{cmax}/I_{co} \qquad (A.1.3.1)$$

This is the ratio of peak to d.c. collector current. By equating I_{cmax} to the Kirk current limit (directly expressable in terms of device physical parameters) we can relate the performance to that of a real device (since the same physical parameters also determine the breakdown voltage of the collector-base junction, V_{cbr}) as can be seen in Appendix 1.2.

Reference [6] also enables the power gain to be calculated

$$G2ALP = 2 P_{in}/I_{B1}^2 r_{bb} \qquad (A.1.3.2)$$

The base resistance r_{bb} is a device parameter, expressed in terms of physical paremeters in Appendix 1.1.

We can relate class C behaviour to existing class A results by using the following equations:

$$G_{pA} = R_{LA}/[(\omega_1 t_f)^2 r_{bb}] \qquad (A.1.3.3)$$

$$G_{pC} = R_{LC}/[(\omega_1 t_f)^2 r_{bb}\ G2ALP] \qquad (A.1.3.4)$$

where G_{pA} and G_{pC} are the class A and class C power gains, respectively, (see [1] for details). Again, we use the results in [6] to relate these two quantities by:

$$GLOSS = G_{pC}/G_{pA} = AI^5/(2.G2ALP) \qquad (A.1.3.5)$$

The various FORTRAN terms are printed in the sample output of Appendix 2. This now provides us with sufficient information to calculate class C power gain, power output and 'low frequency' efficiency (as defined in [6]. We have however, extended the simple analytic treatment to include two additional nigh frequency sources of loss.

Elementary analysis shows that a 'voltage efficiency' (ETAV in the sample output of Appendix 2) can be defined by the breakdown voltage V_{cbr} and the saturation voltage V_{cesat},

$$\eta_v = ETAV = 1 - 2\,V_{cesat}/V_{cbr} \qquad (A.1.3.6)$$

From the physical properties of the collector epitaxial layer, this can be expressed as:

$$ETAV = 1 - 4\,E_c/E_{br} \qquad (A.1.3.7)$$

where E_c is the 'critical field' ($\simeq 10^4$V/cm in silicon) and E_{br} is the breakdown value of field ($\simeq 10^5$ to 10^6 V/cm in silicon). Note that this is a 'low frequency efficiency' but that use of the full epitaxial layer resistance in converting (A.1.3.6) to (A.1.3.7) renders the result valid at high frequencies (maximum current equal to the Kirk current I_K has been assumed in the derivation).

Reference [4] gives some power gain and efficiency results taking high frequency waveforms into account. A normalised parameter, ν, is defined as:

$$\nu = \omega_s C_{je} (R_g + r_{bb}) \qquad (A.1.3.8)$$

where C_{je} is the emitter-base capacitance. We have re-arranged this formula as follows:

$$NU = FC(f_t/f_s)(1 + R_{in}/r_{bb})/4G_{pC} \qquad (A.1.3.9)$$

where FC is the ratio of emitter-base depletion layer capacitance to collector-base capacitance (of order 10 for typical transistors), f_t is the transition frequency and f_s the signal frequency. The ratio R_{in}/r_{bb} is obtained for each case from the preceding equations [6]. To determine the corresponding efficiency and power gain in this simplified study, the following empirical expressions were 'fitted' to the curves given in [4]:

$$ETANU = (1 - 2.NU(1 - ETA))ETA \qquad (A.1.3.10)$$

$$GDBNU = 2.GDBA.\exp(-NU)/(1 + \exp(-NU)) + 1 \qquad (A.1.3.11)$$

We stress here that the sole purpose is to obtain a first order approximation to real performance to enable preliminary design data to be obtained.

Finally, to take account of the loss due to the capacitive current (from C_{jc}) flowing in the collector (epitaxial) series resistance, the following relations apply:

$$i = \omega_s C V_o$$

$$P_{loss} = i^2 R_c$$

where P_{loss} is the power loss in the resistance R_c. Since the useful output power is $P_{out} = V_o^2/R_L$ we can define a 'loss factor'

$$FLOSS = P_{loss}/P_{out} = K(\omega_s C R_c)^2 (R_L/R_c) \qquad (A.1.3.12)$$

Expressing the collector capacitance and resistance in terms of the epitaxial layer parameters enables us to write:

$$FLOSS = 5.7(\omega_s \tau_{rel})^2 . A/5 . V_{cbr}/(2V_{cesat}\eta_i) \qquad (A.1.3.13)$$

where τ_{rel} is the dielectric relaxation time ($\rho\varepsilon$) of the epitaxial layer and ω_s is the signal frequency in radians/s; the remaining terms have been defined above. The corresponding component of efficiency may now be expressed as:

$$ETA(F) = ETA(1 - FLOSS) \qquad (A.1.3.14)$$

where ETA is the product of low frequency 'voltage' and 'current' efficiencies η_v, η_i discussed above.

In the output given in full in [1] and [2] and of which we include a sample in Appendix 2, we have defined the expected overall efficiency (plotted in Fig.1) by:

$$ETAO = 1/[(1/ETAN') + FLOSS] \qquad (A.1.3.15)$$

This includes all the low and high frequency sources of loss mentioned above, in an empirical manner, but of sufficient accuracy for the purpose of choosing initial design parameters and even of estimating initial operating conditions (conduction angle, etc.).

GRAS RESULTS FOR 2ALPH = 100. PSIC = 0.25E 00 GAIN = 0.20E 02 PINJ = 0.10E 02

A15	A16	G2ALP	A19	A18	M.MATCH	GLOSS	FVCB	FCJC	FC	FAFT
0.72E 01	0.12E 02	0.29E 02	0.11E 02	0.15E 00	0.243E 00	0.122E 00	1.0	4.0	10.0	2.0

FTN	WB	NEPI	VCBR	ETAI	ETAN	ETAFN	GDBN	GDBN	
FNO	WEPI	NBMIN	VCSAT	ETAV	ETA	ETA(F)	FLOSS	NU	FT(REAL)
0.490E 10	0.477E-04	0.459E 16	0.774E 02	0.950	0.821	0.806	0.130E 02	0.46E 01	
0.313E 11	0.459E-03	0.442E 17	0.656E 00	0.983	0.934	0.915	0.227E-01	0.18E 01	0.25E 10

ELEM	RBESQ	RBESQA	IMAX	ICO	GDBA	GDBNU	NUA	FNOA	ETANU	ETAO
0.10E-03	0.19E 05	0.93E 04	0.73E 00	0.10E 00	16.2	10.5	0.883E 00	0.453E 11	0.880	0.863
0.15E-03	0.86E 04	0.86E 04	0.11E 01	0.15E 00	13.0	4.6	0.184E 01	0.313E 11	0.821	0.806
0.20E-03	0.48E 04	0.48E 04	0.15E 01	0.20E 00	13.0	4.6	0.184E 01	0.313E 11	0.821	0.806
0.30E-03	0.21E 04	0.21E 04	0.22E 01	0.31E 00	13.0	4.6	0.184E 01	0.313E 11	0.821	0.806
0.40E-03	0.12E 04	0.12E 04	0.29E 01	0.41E 00	13.0	4.6	0.184E 01	0.313E 11	0.821	0.806

FTN	WB	NEPI	VCBR	ETAI	ETAN	ETAFN	GDBN	GDBN	
FNO	WEPI	NBMIN	VCSAT	ETAV	ETA	ETA(F)	FLOSS	NU	FT(REAL)
0.980E 10	0.337E-04	0.109E 17	0.460E 02	0.950	0.828	0.824	0.130E 02	0.46E 01	
0.313E 11	0.230E-03	0.743E 17	0.328E 00	0.986	0.937	0.933	0.477E-02	0.18E 01	0.45E 10

ELEM	RBESQ	RBESQA	IMAX	ICO	GDBA	GDBNU	NUA	FNOA	ETANU	ETAO
0.10E-03	0.19E 05	0.78E 04	0.17E 01	0.24E 00	17.0	11.9	0.742E 00	0.494E 11	0.893	0.889
0.15E-03	0.86E 04	0.78E 04	0.26E 01	0.36E 00	13.4	5.3	0.167E 01	0.329E 11	0.838	0.834
0.20E-03	0.48E 04	0.48E 04	0.35E 01	0.48E 00	13.0	4.6	0.184E 01	0.313E 11	0.828	0.824
0.30E-03	0.21E 04	0.21E 04	0.52E 01	0.73E 00	13.0	4.6	0.184E 01	0.313E 11	0.828	0.824
0.40E-03	0.12E 04	0.12E 04	0.70E 01	0.97E 00	13.0	4.6	0.184E 01	0.313E 11	0.828	0.824

FTN	WB	NEPI	VCBR	ETAI	ETAN	ETAFN	GDBN	GDBN	
FNO	WEPI	NBMIN	VCSAT	ETAV	ETA	ETA(F)	FLOSS	NU	FT(REAL)
0.196E 11	0.238E-04	0.259E 17	0.274E 02	0.950	0.833	0.833	0.130E 02	0.46E 01	
0.313E 11	0.115E-03	0.125E 18	0.164E 00	0.988	0.939	0.938	0.1C0E-02	0.18E 01	0.98E 10

ELEM	RBESQ	RBESQA	IMAX	ICO	GDBA	GDBNU	NUA	FNOA	ETANU	ETAO
0.10E-03	0.19E 05	0.66E 04	0.42E 01	0.58E 00	17.7	13.4	0.625E 00	0.538E 11	0.903	0.902
0.15E-03	0.86E 04	0.66E 04	0.62E 01	0.86E 00	14.2	6.6	0.141E 01	0.359E 11	0.858	0.858
0.20E-03	0.48E 04	0.48E 04	0.83E 01	0.12E 01	13.0	4.6	0.184E 01	0.313E 11	0.833	0.833
0.30E-03	0.21E 04	0.21E 04	0.12E 02	0.17E 01	13.0	4.6	0.184E 01	0.313E 11	0.833	0.833
0.40E-03	0.12E 04	0.12E 04	0.17E 02	0.23E 01	13.0	4.6	0.184E 01	0.313E 11	0.833	0.833

FTN	WB	NEPI	VCBR	ETAI	ETAN	ETAFN	GDBN	GDBN	
FNO	WEPI	NBMIN	VCSAT	ETAV	ETA	ETA(F)	FLOSS	NU	FT(REAL)
0.392E 11	0.169E-04	0.614E 17	0.162E 02	0.950	0.838	0.838	0.130E 02	0.46E 01	
0.313E 11	0.574E-04	0.209E 18	0.820E-01	0.990	0.941	0.941	0.212E-03	0.18E 01	0.20E 11

ELEM	RBESQ	RBESQA	IMAX	ICO	GDBA	GDBNU	NUA	FNOA	ETANU	ETAO
0.10E-03	0.19E 05	0.55E 04	0.98E 01	0.14E 01	18.4	14.7	0.527E 00	0.586E 11	0.911	0.911
0.15E-03	0.86E 04	0.55E 04	0.15E 02	0.20E 01	14.9	8.0	0.119E 01	0.391E 11	0.875	0.874
0.20E-03	0.48E 04	0.48E 04	0.20E 02	0.27E 01	13.0	4.6	0.184E 01	0.313E 11	0.838	0.838
0.30E-03	0.21E 04	0.21E 04	0.29E 02	0.41E 01	13.0	4.6	0.184E 01	0.313E 11	0.838	0.838
0.40E-03	0.12E 04	0.12E 04	0.39E 02	0.55E 01	13.0	4.6	0.184E 01	0.313E 11	0.838	0.838

Appendix 2: Computer output for $\theta = 100^0$ for analytic design (Sample reproduced from [2]).

Appendix 3: Sample BIPOLE output

We enclose one sample output from the BIPOLE program. Since the detailed output for the SP9S1, SP2S2 and SP2A2 transistors (and others) was included in earlier reports, we have chosen as our example here, the output corresponding to the GaAs transistor used in the WATAND studies presented in this report, but modified by an additional base diffusion near the surface to reduce the extrinsic component of base resistance (see section 8 of this report). The emitter concentration close to the surface was simultaneously increased (necessarily).

In the following 7 pages of BIPOLE output, the following are the parameters and comments of particular relevance to this study:

page 2: The input profile data (see Fig.2?) is printed

The three sheet resistances (cf table 1) resulting from integration of the impurity profile are printed (RB, RE, RBE OHM/SQ)

The various breakdown voltages computed from the ionization integral

The zero bias junction capacitances.

page 3: This is a printer plot of the separate donor and acceptor atom profiles.

page 4: This is the result of the vertical one dimensional solution of the transport and Poisson equations. Of particular significance are :

- TBASE the neutral base region transit time
- TSCL the collector-base space charge layer delay time
- TEM the delay time due to the excess charge in the neutral emitter
- FTOT the (one dimensional) overall value of f_t (transition frequency)
- FMAX the value of FTOT neglecting the effect of junction capacitances

page 5: This is the result of the horizontal integration of the base transport equation. The main parameters of importance in this study are:

- FT the overall value of transition frequency f_t (note that this is lower than the one dimensional analysis value, due to edge junction effects).
- FMOSC the maximum oscillation (unity power gain) frequency
- IC the d.c. collector current

page 6: printer plot of current gain h_{FE} (BETA)

page 7: printer plot of transition frequency f_t

page 8: Gummel-Poon and Extended Ebers-Moll CAD model parameters. Note the reduction in extrinsic base resistance RBEX compared to the SP2A2 design.

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NOV. 2?  1978      16:18:04              BIP VERSION  1/11/78 V.10.05
FILE NAME: SP2A?

*****************************************************************************
*                                                                           *
*                                                                           *
*          BIPOLAR DEVICE ANALYSIS AND MODEL GENERATION PROGRAMME           *
*                                                                           *
*                                                                           *
*             BIPOLE VERSION V.10.04,  CREATED 01 NOV   1978                *
*                                                                           *
*                                                                           *
*****************************************************************************

  GAAS     NPN     TRANSISTOR AT TEMPERATURE OF   27. DEGREES C (NI = 0.11E+08)

MASK DATA       ELE4        B          ESB         ECB         BPB        ELPB
             0.150E-03 0.133E+01 0.150E-03 0.150E-03 0.140E+01 0.700E-03

PROFILE DATA  NE1       NB1       NEPI      XE1       XB1       XEPI    NXE1 NXB1
         0.200E+19 0.100E+01 0.250E+17 0.162E-04 0.324E-04 0.200E-03    6    2

NON GAUSSIAN EMITTER PROFILE: NE2 = 0.100E+22 XE2 = 0.700E-05 NXE2 =  6

NON GAUSSIAN BASE PROFILE:    NB2 = 0.500E+20 XB2 = 0.700E-05 NXB2 =  6

IMPLANTED BASE PROFILE OF 0.20E+19 AT X = 0.22E-04 FOR XBIM = 0.1CE-04 NXEIM = 2

EMPIRICALLY DERIVED VOLTAGE AND CURRENT LIMITS:

   VBPLAN   VBMESA    VBEPI     VBEBO   VCESAT(IK)     IK        IHLI       ISAT(10)
 0.234E+02 0.447E+02 0.458E+02 0.560E+01 0.213E+00 0.880E+01 0.446E+02 0.412E+03

PROFILE INTEGRATION FOR XJ1 = 0.147E-04 XJ2 = 0.429E-04 RA = 0.120E+01 NPOINT = 265

RB-OHM/SQ RE-OHM/SQ RBE-OHM/SQ  RBC          RE          RBEXT      REPI  GUMMEL NO
 0.302E+03 0.751E+00 0.218E+04 0.205E-01 C.118E-03 0.171E-01 0.243E-01 0.263E+14

 VBR =-0.750E+01 + OR -  0. %, X = 0.210E-04 (IONIZATION INTEGRAL FOR PLANE JUNCTION)  1

 VBR = 0.321E+02 + OR - 10. %, X = 0.165E-03 (IONIZATION INTEGRAL FOR PLANE JUNCTION)  2

 VBR = 0.197E+02 + OR - 50. %, X = 0.107E-04 (IONIZATION INTEGRAL FOR PERIPHERAL JUNCTION )  1

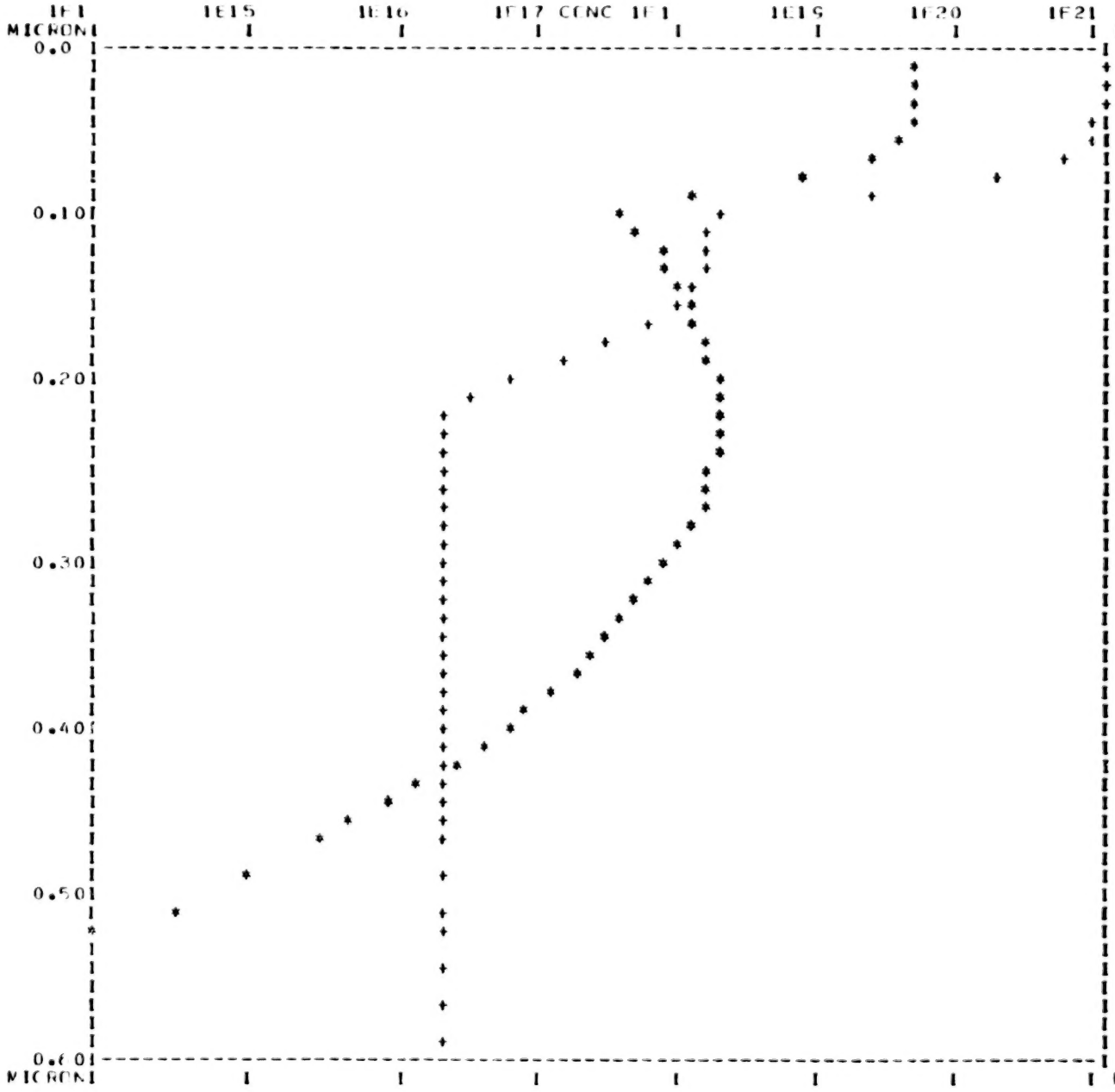
CJE(EDGE)= 0.331E-10 F/CM(PERIPHERY). CJE(PLANE)= 0.154E-06 F/SQ.CM, FOR VBE=0

CJC(EDGE)= 0.0        F/CM(PERIPHERY). CJC(PLANE)= 0.360E-07 F/SQ.CM, FOR VCB=0

CAPACITANCES AT ZERO BIAS: CJEO = 0.119E-09 CJCC = 0.353E-10  ECE = 0.929E+01

ECJE = 0.286E+01 ECJC = 0.390E+01 ECJCO = 0.350E+01

VIOEP=1.323 VICCO=1.172 XBC = 0.367E-04 XCC = 0.644E-04 RHO(EPI)=  0.038 OHM-CM
```



MICRON	CONC	CONC
0.02	0.50E+20	0.10E+22
0.03	0.50E+20	0.10E+22
0.03	0.49E+20	0.99E+21
0.05	0.44E+20	0.88E+21
0.06	0.37E+20	0.74E+21
0.07	0.24E+20	0.49E+21
0.08	0.85E+19	0.17E+21
0.09	0.15E+19	0.25E+20
0.10	0.48E+18	0.22E+19
0.11	0.59E+19	0.18E+19
0.13	0.82E+18	0.16E+19
0.13	0.91E+18	0.15E+19
0.14	0.11E+19	0.13E+19
0.15	0.13E+19	0.10E+19
0.16	0.15E+19	0.71E+18
0.18	0.17E+19	0.39E+18
0.19	0.18E+19	0.19E+18
0.20	0.19E+19	0.71E+17
0.21	0.20E+19	0.42E+17
0.23	0.20E+19	0.26E+17
0.23	0.20E+19	0.25E+17
0.24	0.19E+19	0.25E+17
0.26	0.17E+19	0.25E+17
0.27	0.16E+19	0.25E+17
0.27	0.15E+19	0.25E+17
0.29	0.12E+19	0.25E+17
0.30	0.11E+19	0.25E+17
0.31	0.92E+18	0.25E+17
0.32	0.76E+18	0.25E+17
0.33	0.58E+18	0.25E+17
0.34	0.48E+18	0.25E+17
0.35	0.37E+18	0.25E+17
0.36	0.26E+18	0.25E+17
0.37	0.20E+18	0.25E+17
0.38	0.14E+18	0.25E+17
0.39	0.95E+17	0.25E+17
0.40	0.69E+17	0.25E+17
0.41	0.45E+17	0.25E+17
0.43	0.29E+17	0.25E+17
0.44	0.18E+17	0.25E+17
0.45	0.11E+17	0.25E+17
0.46	0.57E+16	0.25E+17
0.47	0.32E+16	0.25E+17
0.49	0.11E+16	0.25E+17
0.51	0.36E+15	0.25E+17
0.53	0.11E+15	0.25E+17
0.55	0.29E+14	0.25E+17
0.57	0.74E+13	0.25E+17
0.59	0.17E+13	0.25E+17
MICRON	CONC	CONC

TR LY (0 DI .10 .) I JLT_ DE' IN 15.... ..4 = ..36 . FACN = . .

NJ NJ	NU ITC	JN JP	BETAE BETAT	VBE M	IBE ND(0)	TEN VCB	TBASE WB	ISCL WSCL	IBC RBB	ETOT FMAX	NC PD
1	15	0.293E+03	0.919E+01	0.112E+01	0.27E-10	0.11E-11	0.29E-11	0.58E-11	0.23E-13	0.43E+10	0.10E+16
1	12	-0.319E+02	0.499E+01	0.100E+01	-0.66E+18	0.20E+02	0.18E-04	0.14E-03	0.24E-01	0.16E+11	0.11E+16
2	6	0.587E+03	0.442E+01	0.114E+01	0.15E-10	0.12E-11	0.30E-11	0.59E-11	0.22E-13	0.63E+10	0.22E+16
2	7	-0.697E+02	0.428E+01	0.109E+01	-0.64E+18	0.21E+02	0.18E-04	0.14E-03	0.24E-01	0.16E+11	0.24E+16
3	8	0.117E+04	0.125E+02	0.116E+01	0.87E-11	0.12E-11	0.32E-11	0.59E-11	0.22E-13	0.84E+10	0.53E+16
3	12	-0.940E+02	0.123E+02	0.121E+01	-0.62E+18	0.20E+02	0.18E-04	0.14E-03	0.23E-01	0.15E+11	0.57E+16
4	15	0.235E+04	0.123E+02	0.118E+01	0.35E-11	0.12E-11	0.32E-11	0.60E-11	0.22E-13	0.11E+11	0.11E+17
4	7	-0.190E+03	0.122E+02	0.938E+00	-0.59E+18	0.20E+02	0.18E-04	0.14E-03	0.23E-01	0.15E+11	0.11E+17
5	10	0.469E+04	0.120E+02	0.119E+01	0.18E-11	0.12E-11	0.32E-11	0.61E-11	0.20E-13	0.13E+11	0.21E+17
5	7	-0.391E+03	0.119E+02	0.935E+00	-0.57E+18	0.20E+02	0.18E-04	0.14E-03	0.23E-01	0.15E+11	0.22E+17
6	20	0.939E+04	0.115E+02	0.121E+01	0.96E-12	0.12E-11	0.32E-11	0.72E-11	0.11E-13	0.13E+11	0.40E+17
6	7	-0.818E+03	0.114E+02	0.935E+00	-0.55E+18	0.24E+02	0.18E-04	0.16E-03	0.23E-01	0.14E+11	0.43E+17
7	28	0.188E+05	0.981E+01	0.123E+01	0.57E-12	0.13E-11	0.33E-11	0.93E-11	0.15E-14	0.11E+11	0.82E+17
7	8	-0.191E+04	0.978E+01	0.105E+01	-0.52E+18	0.36E+02	0.18E-04	0.20E-03	0.23E-01	0.11E+11	0.86E+17
8	21	0.375E+05	0.115E+02	0.125E+01	0.30E-12	0.13E-11	0.34E-11	0.93E-11	0.15E-14	0.11E+11	0.16E+18
8	6	-0.325E+04	0.115E+02	0.104E+01	-0.50E+18	0.66E+02	0.18E-04	0.20E-03	0.22E-01	0.11E+11	0.16E+18
9	5	0.751E+05	0.837E+01	0.127E+01	0.18E-12	0.15E-11	0.28E-10	0.44E-11	0.31E-14	0.47E+10	0.30E+18
9	10	-0.897E+04	0.835E+01	0.116E+01	-0.46E+18	0.15E+02	0.11E-03	0.20E-03	0.10E-01	0.47E+10	0.31E+18
10	4	0.150E+06	0.546E+01	0.130E+01	0.12E-12	0.19E-11	0.41E-10	0.30E-11	0.47E-14	0.34E+10	0.61E+18
10	11	-0.275E+05	0.545E+01	0.144E+01	-0.42E+18	0.19E+02	0.13E-03	0.20E-03	0.46E-02	0.34E+10	0.62E+18

*** NON-CONVERGENCE 3 TIMES. VCAV = 0.248E+02 VCMAX = 0.645E+02 VCMIN = 0.136E+02

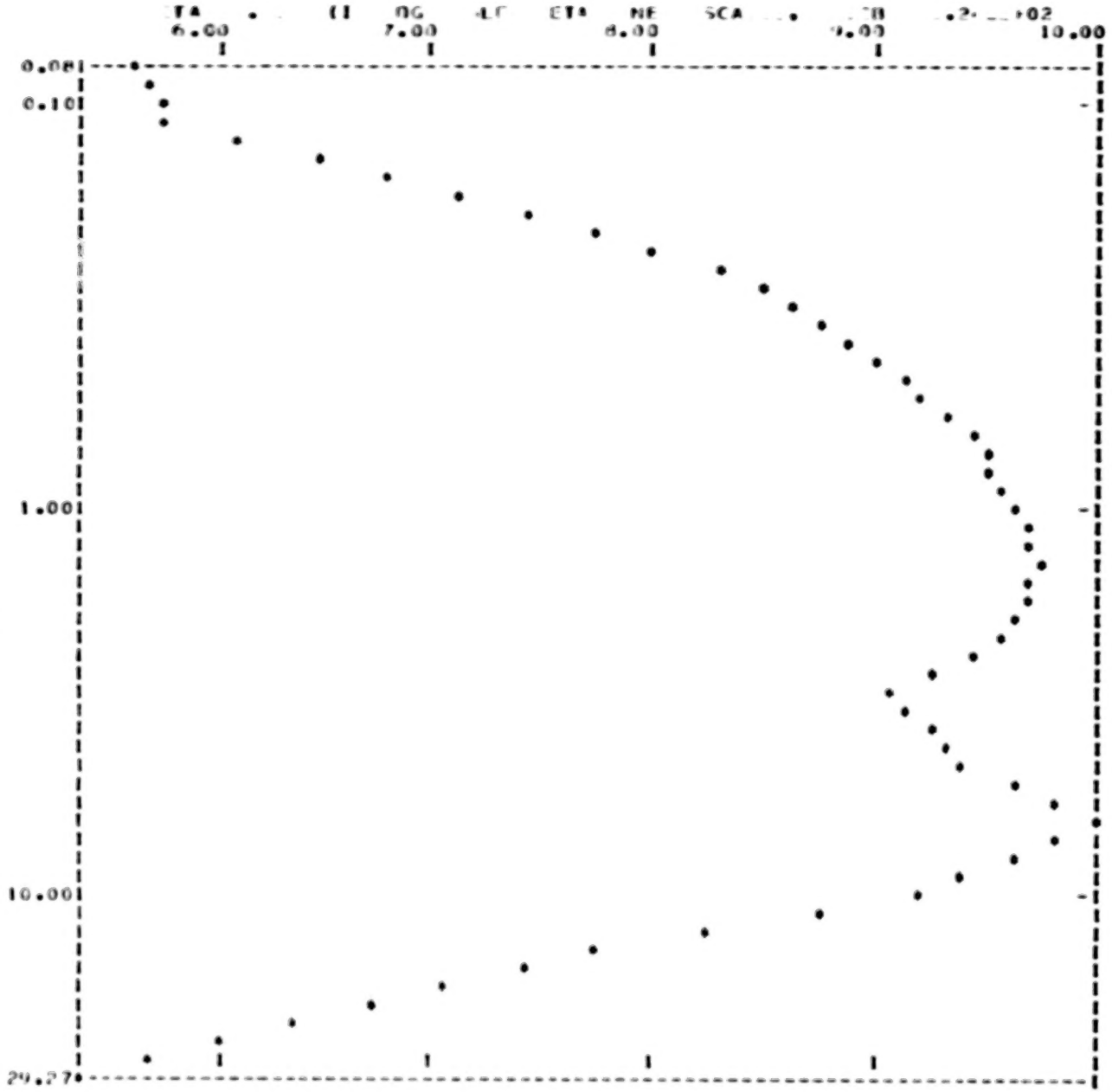
GIVEN: TAUE = 0.100E-08 TAUB = 0.100E-06 TAUC = 0.100E-05

BETAI (INFINITE TAUP) = 0.928E+01 BETMAX = 0.121E+02

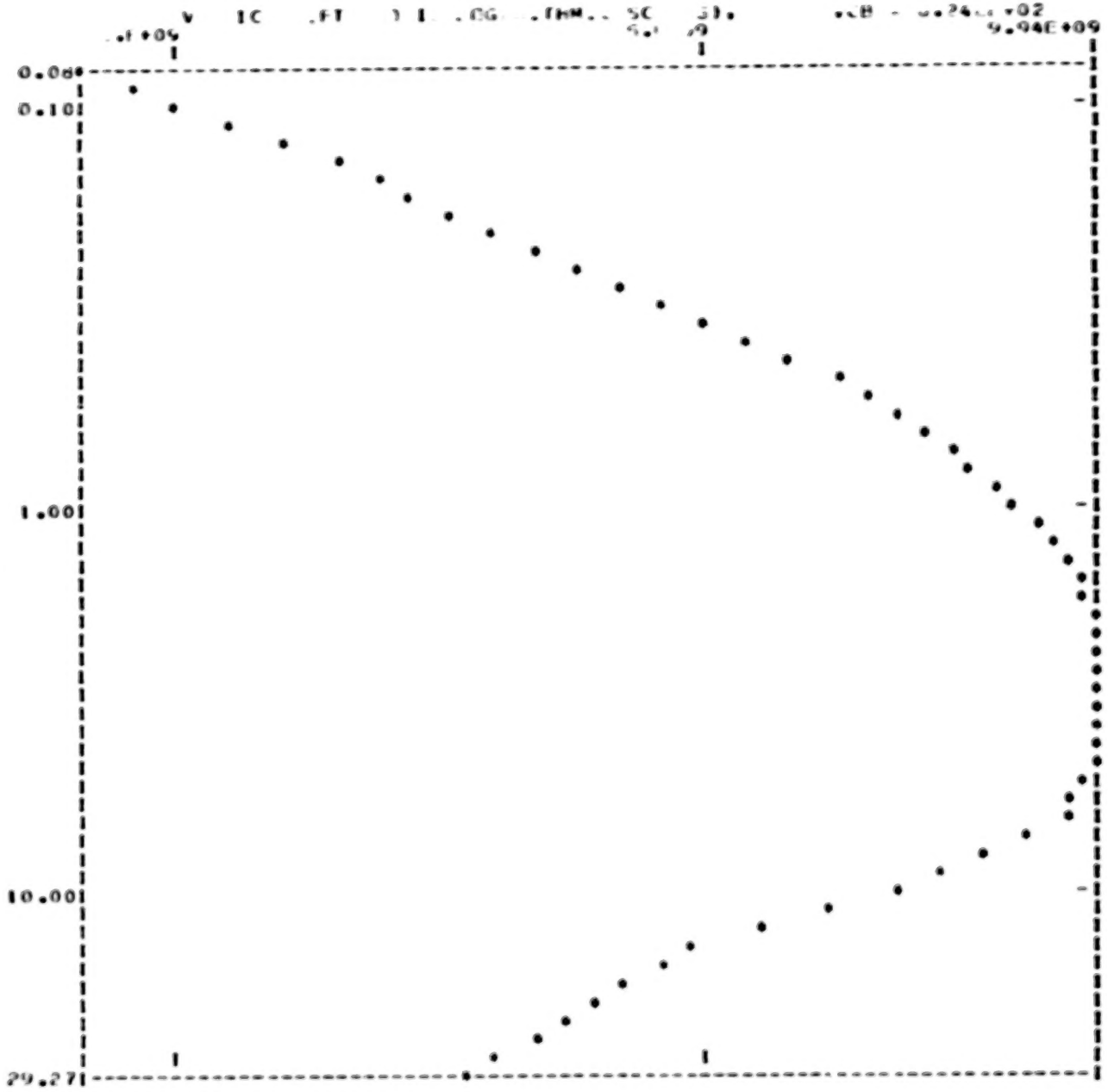
PBASE = 0.238E-01 REAL GUMMEL NO. = 0.240E+14 VBCEO (APPROX) = 0.140E+02

GAIN LIMIT DUE TO E-B DIODE, BEED = 0.104E-07

0.790E-01	0.113E+01	0.566E+01	0.171E+10	0.140E-01	0.392E-01	0.997E+00	0.396E+03	
0.790E-01	0.296E+01	0.612E+01	0.113E+11	0.234E+01	0.237E-05	0.951E-11	0.772E-10	
0.107E+00	0.114E+01	0.578E+01	0.220E+10	0.188E-01	0.389E-01	0.996E+00	0.539E+03	
0.107E+00	0.319E+01	0.612E+01	0.126E+11	0.324E+01	0.241E-05	0.945E-11	0.865E-10	
0.141E+00	0.115E+01	0.644E+01	0.270E+10	0.218E-01	0.388E-01	0.994E+00	0.706E+03	
0.141E+00	0.417E+01	0.102E+02	0.143E+11	0.422E+01	0.243E-05	0.939E-11	0.998E-10	
0.184E+00	0.115E+01	0.739E+01	0.326E+10	0.249E-01	0.384E-01	0.992E+00	0.926E+03	
0.184E+00	0.454E+01	0.142E+02	0.157E+11	0.457E+01	0.247E-05	0.934E-11	0.107E-09	
0.247E+00	0.116E+01	0.831E+01	0.403E+10	0.297E-01	0.350E-01	0.987E+00	0.125E+04	
0.247E+00	0.814E+01	0.131E+02	0.190E+11	0.819E+01	0.251E-05	0.928E-11	0.152E-09	
0.348E+00	0.117E+01	0.875E+01	0.503E+10	0.397E-01	0.347E-01	0.982E+00	0.177E+04	
0.348E+00	0.111E+02	0.101E+02	0.202E+11	0.115E+02	0.256E-05	0.945E-11	0.185E-09	
0.492E+00	0.118E+01	0.911E+01	0.637E+10	0.540E-01	0.342E-01	0.975E+00	0.252E+04	
0.492E+00	0.179E+02	0.101E+02	0.228E+11	0.188E+02	0.262E-05	0.948E-11	0.249E-09	
0.701E+00	0.119E+01	0.943E+01	0.749E+10	0.744E-01	0.337E-01	0.965E+00	0.363E+04	
0.701E+00	0.220E+02	0.103E+02	0.249E+11	0.235E+02	0.268E-05	0.945E-11	0.291E-09	
0.100E+01	0.120E+01	0.964E+01	0.869E+10	0.104E+00	0.328E-01	0.953E+00	0.534E+04	
0.100E+01	0.347E+02	0.102E+02	0.272E+11	0.383E+02	0.275E-05	0.940E-11	0.431E-09	
0.145E+01	0.121E+01	0.975E+01	0.947E+10	0.149E+00	0.319E-01	0.913E+00	0.796E+04	
0.145E+01	0.434E+02	0.999E+01	0.288E+11	0.453E+02	0.282E-05	0.926E-11	0.544E-09	
0.210E+01	0.122E+01	0.959E+01	0.994E+10	0.219E+00	0.304E-01	0.884E+00	0.119E+05	
0.210E+01	0.655E+02	0.927E+01	0.303E+11	0.799E+02	0.290E-05	0.906E-11	0.843E-09	
0.303E+01	0.122E+01	0.905E+01	0.985E+10	0.335E+00	0.287E-01	0.822E+00	0.184E+05	
0.303E+01	0.725E+02	0.801E+01	0.310E+11	0.932E+02	0.297E-05	0.892E-11	0.101E-08	
0.452E+01	0.124E+01	0.940E+01	0.983E+10	0.481E+00	0.272E-01	0.745E+00	0.303E+05	
0.452E+01	0.116E+03	0.102E+02	0.317E+11	0.157E+03	0.307E-05	0.879E-11	0.167E-08	
0.670E+01	0.126E+01	0.100E+02	0.947E+10	0.676E+00	0.225E-01	0.712E+00	0.475E+05	
0.670E+01	0.184E+03	0.115E+02	0.328E+11	0.223E+03	0.316E-05	0.894E-11	0.285E-08	
0.984E+01	0.127E+01	0.921E+01	0.705E+10	0.107E+01	0.143E-01	0.714E+00	0.690E+05	
0.984E+01	0.258E+03	0.783E+01	0.312E+11	0.265E+03	0.327E-05	0.920E-11	0.551E-08	
0.143E+02	0.128E+01	0.773E+01	0.459E+10	0.184E+01	0.870E-02	0.713E+00	0.100E+06	
0.143E+02	0.352E+03	0.569E+01	0.277E+11	0.381E+03	0.339E-05	0.971E-11	0.110E-07	
0.204E+02	0.129E+01	0.635E+01	0.398E+10	0.321E+01	0.533E-02	0.695E+00	0.146E+06	
0.204E+02	0.406E+03	0.448E+01	0.258E+11	0.441E+03	0.353E-05	0.106E-10	0.159E-07	
0.293E+02	0.131E+01	0.539E+01	0.332E+10	0.544E+01	0.344E-02	0.676E+00	0.217E+06	
0.293E+02	0.533E+03	0.400E+01	0.248E+11	0.592E+03	0.372E-05	0.114E-10	0.251E-07	



Appendix 3, page 6


0.08
0.10
1.00
10.00
29.27
9.94E+09

CHARGE DISTRIBUTION TABLE

VBFSAT	VCRIT	QFBAS	QBFSAT	QCSAT	QDRSAT	TFBAS	TRBAS
0.112E+01	0.111E+01	0.172E-12	0.974E-12	0.935E-09	0.155E-11	0.294E-11	0.166E-10

VALUES OF 3 IC CURRENTS USED: (VCB = 0.150E+02) FOR MODEL PARAMETER DETERMINATION

	IC1	IC2	IC3
IC	0.589E-01	0.67eE+01	0.204E+02
BETA	0.552E+01	0.100E+02	0.635E+01
RB	0.395E-01	0.225E-01	0.513E-02
RT	0.136E+10	0.947E+10	0.398E+10
VBE	0.112E+01	0.126E+01	0.129E+01

REFERENCE VOLTAGES USED FOR VA AND VB EVALUATION: VGUC = 0.585E+01, VCUE = 0.201E+01

GUMMEL-POON MODEL PARAMETERS FOLLOW

BF	IS	ISS	NSS	IKF	VA	TF	CEO	VPHIF	ME	
BR	ISO	ISR	NSR	IKR	VB	TR	CCO	VPHIC	MC	
ALFCC	RB	RBB	RC	RCEXT	RE					
0.991E+01	0.97CE-20	0.107E-11	0.200E+01	C.8R0E+01	0.185E+03	0.97EL-11	0.119E-09	0.132E+01	0.364E+00	
0.386E+01	0.310E-20	0.252E-12	0.200E+01	0.446E+02	0.239E+02	C.160E-07	0.721E-11	0.117E+01	0.500E+00	
0.390E+01	0.171E-01	0.214E-01	0.159E-01	0.980E-02	0.11RE-03					

BIPOLE GENERATED EBERS-MOLL PARAMETERS FOR WATAND USE

BT IK = 0.758E+00 VBCOR = 3.209E+01

.MI IS 1.950E-21 IF 1.048E+00 TE 300. CS 0.0
GO 3.170E-04 BR 3.719E+00 BF 1.001E+01 C.784E+00 5.520E+00 5.885E-02
0.0 0.0
CE 1.190E-10 0.0 1.323E+00 3.635E-01
CC 3.532E-11 0.0 1.172E+00 4.956E-01
FT 9.467E+09 6.764E+00 1.120E+00 -1.500E+01 TS 1.602E-09
.DATA
RBEXT 1.705E-02
RBB 2.142E-02
RC 1.592E-02
RCEXT 9.797E-03
RE 1.170E-04

EXECUTION TIME= 19.74 SEC.
FILE NAME: SP2A2
NOV. 28, 1978 16:16:04 BIP VERSION 01/11/78 V.10.05

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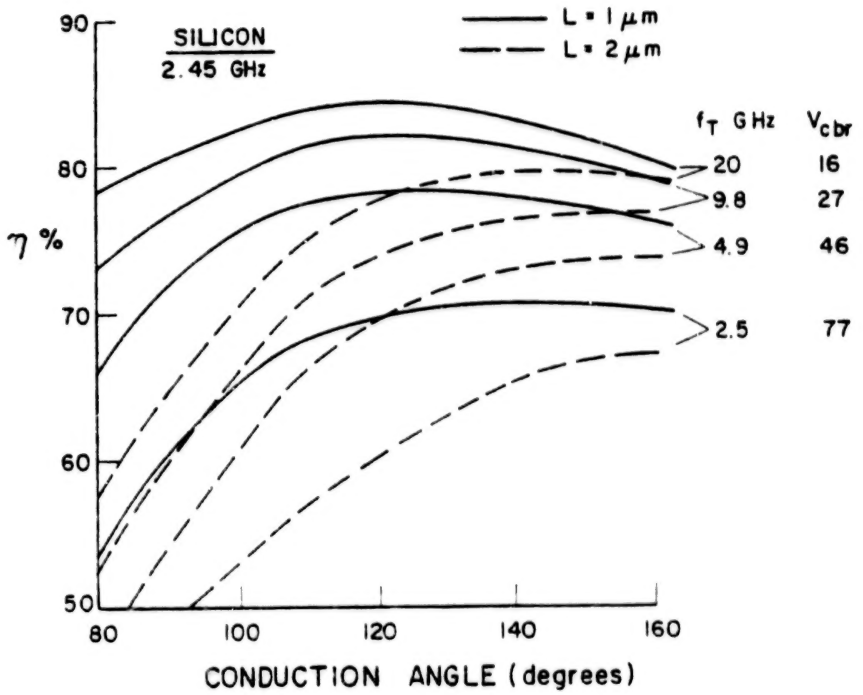
ELLN=1.5E-04,ECC=1.5E-04,ESR=1.5E-04,ELPB=7.0E-04,N=1.331,NPN=1.4,
NEP1=2.5E16,XEP1=2.0E-04,
NE1=2.0E18,XE1=.167E-04,NXE1=6,NN1=1.E00,
NB2=5.0E19,XB2=.070E-04,NXB2=6,
NE2=1.0E21,XE2=.070E-04,NXE2=6,
NPIM=2.0E18,XJEIM=.220E-04,XOIM=0.10E-04,
TAUL=1.E-04,XFS=20.E-04,TAUH=100.E-09,
VCIN=15.,NIOT=IC,
MODEL=4,IPRO=3,DPNIN1=2,XPLMAX=0.6E-04,
&END



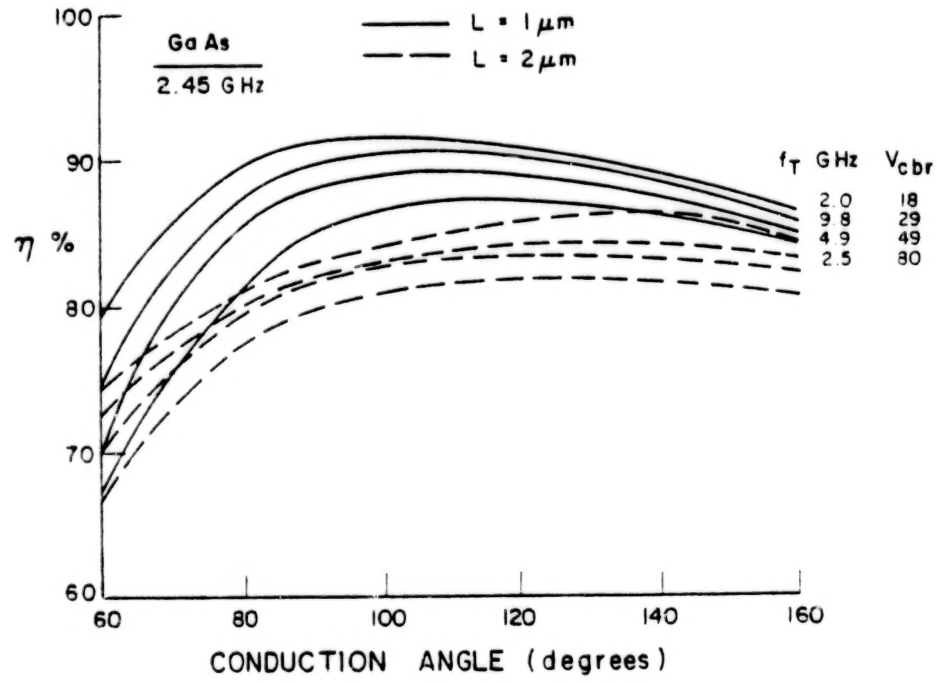


Fig. 1 Efficiency of class C amplifier versus conduction angle θ from semi-empirical analytic analysis. Two values of emitter stripe width, L are shown for both Silicon and GaAs.

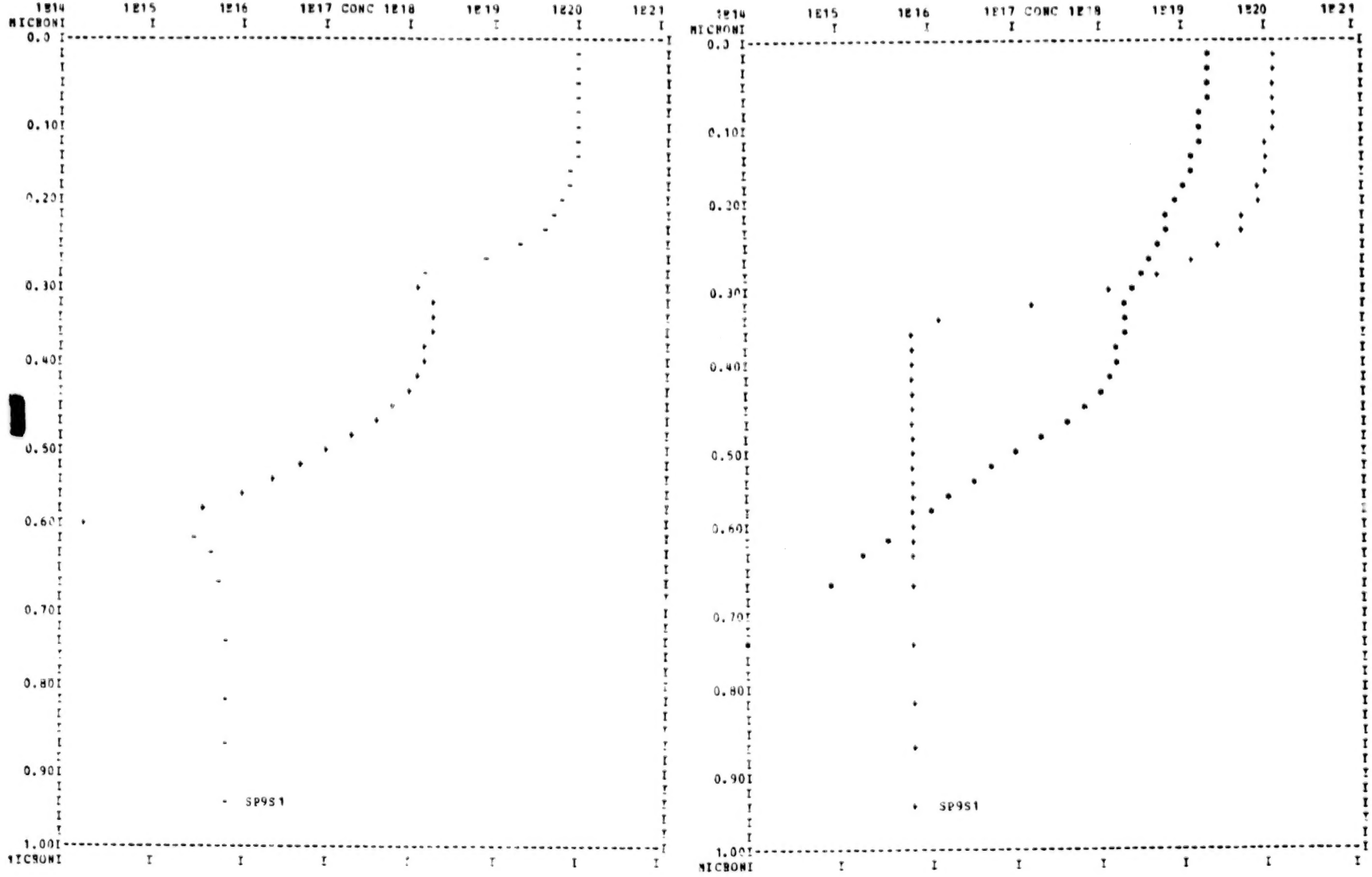


Fig. 2a Final impurity profiles used in the BIPOLE program for the 915 MHz Silicon (SP9S1) transistor (i) net concentration (ii) separate donor and acceptor concentrations.

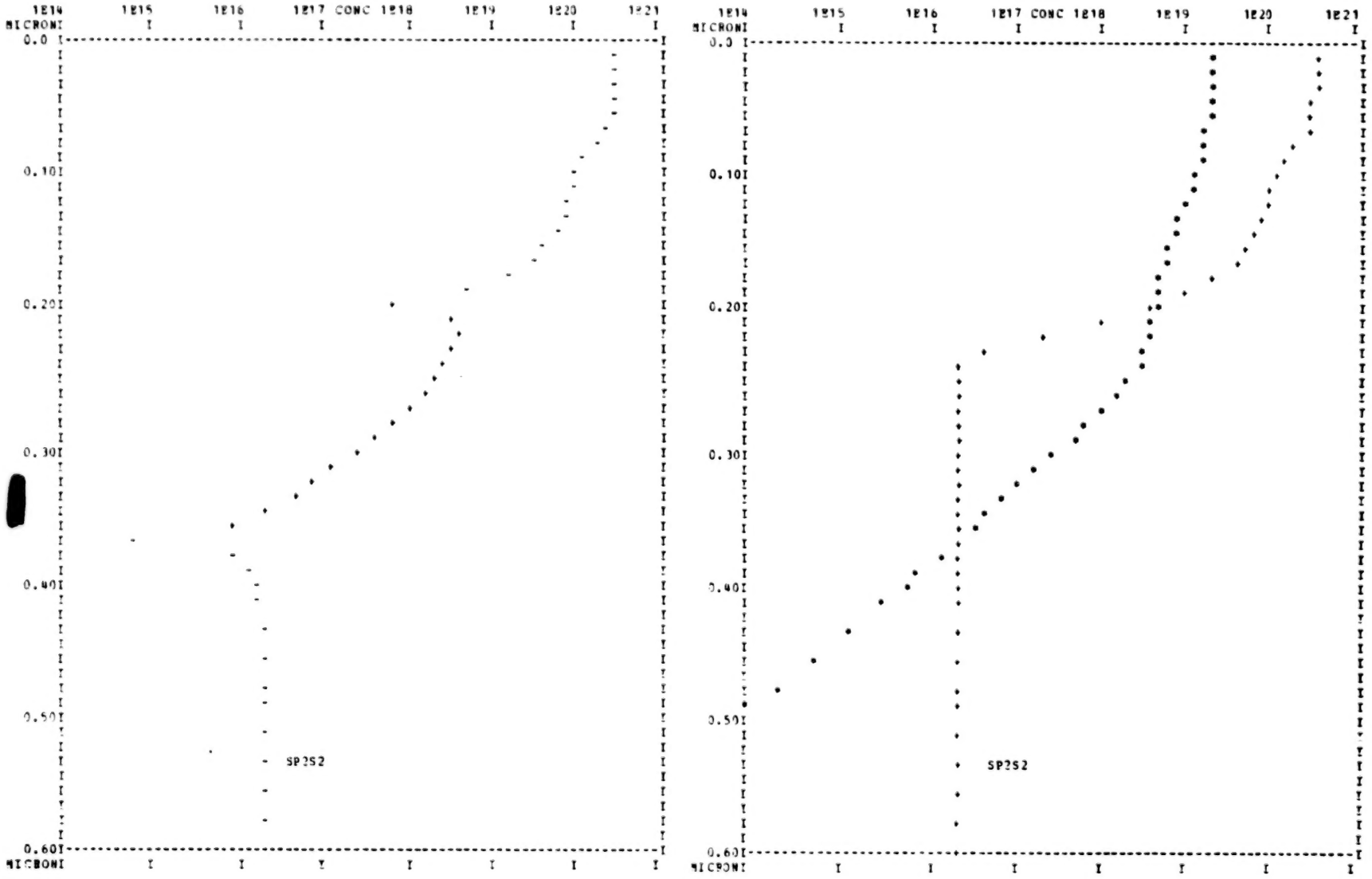


Fig. 2b Final Impurity profiles used in the BIPOLE program for the 2.45 GHz Silicon (SP2S2) transistor (i) net concentration (ii) separate donor and acceptor concentrations.

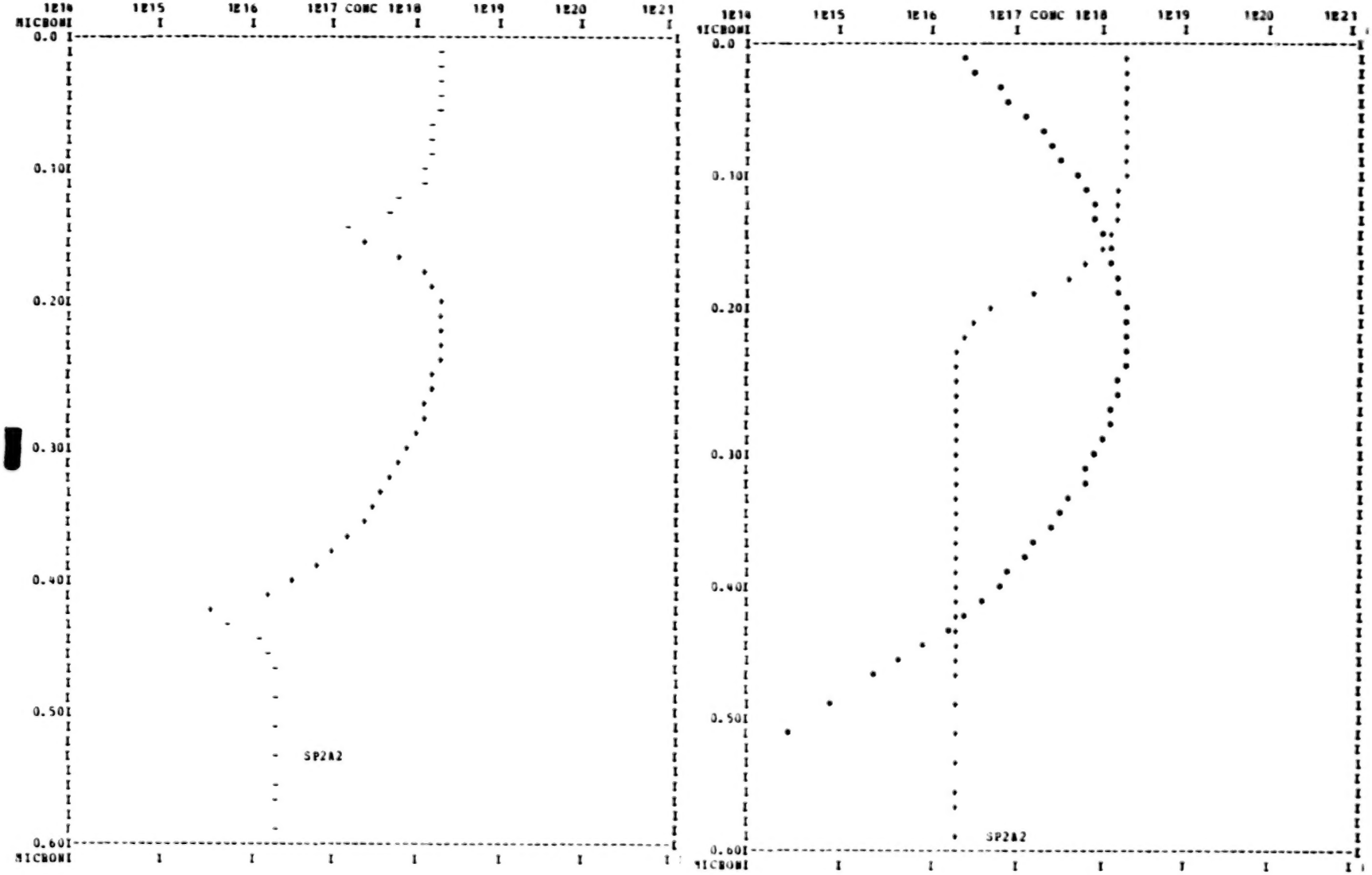


Fig. 2c Final impurity profiles used in the BIPOLE program for the 2.45 GHz GaAs (SP2A2) transistor (i) net concentration (ii) separate donor and acceptor concentrations.

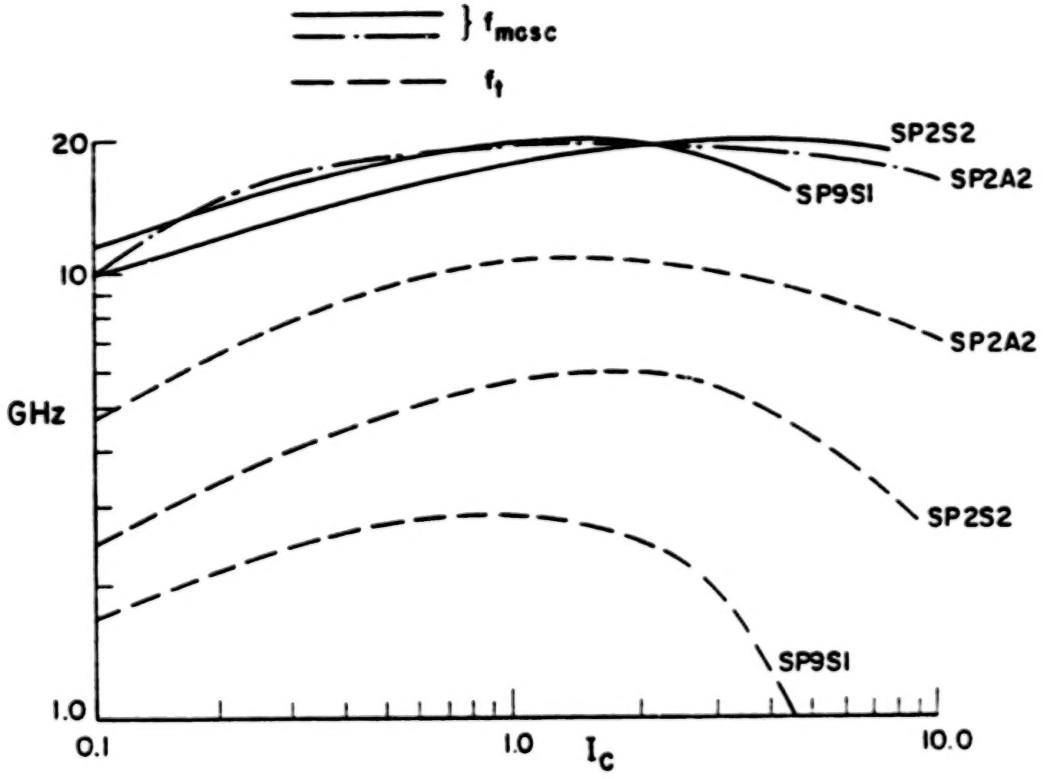


Fig. 3 f_t (transistion frequency) and f_{mosc} (maximum oscillation frequency) computed by the BIPOLE program as a function of d.c. collector current I_c for the three final designs.

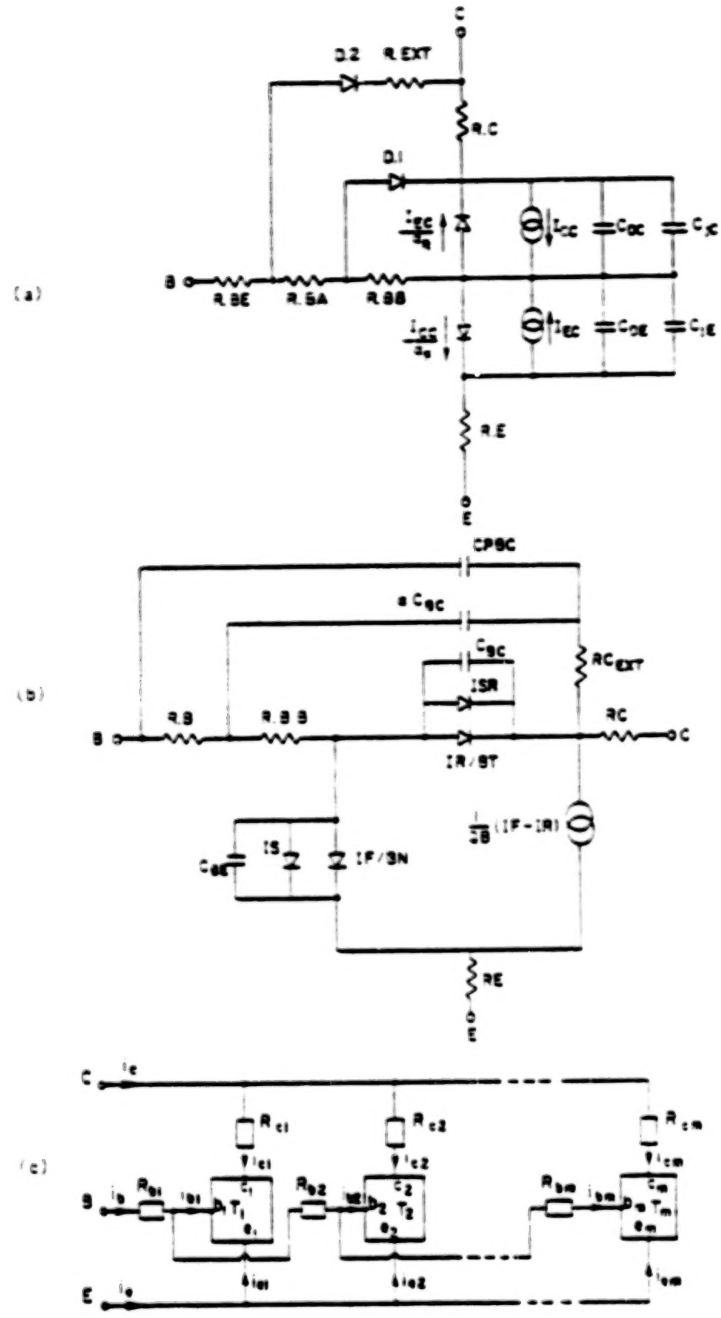


Fig. 4a Extended and modified Ebers-Moll model used in this study.

Fig. 4b Modified Gummel-Poon model used in this study.

Fig. 4c BIPOLE-WATAND tabular model used in this study.

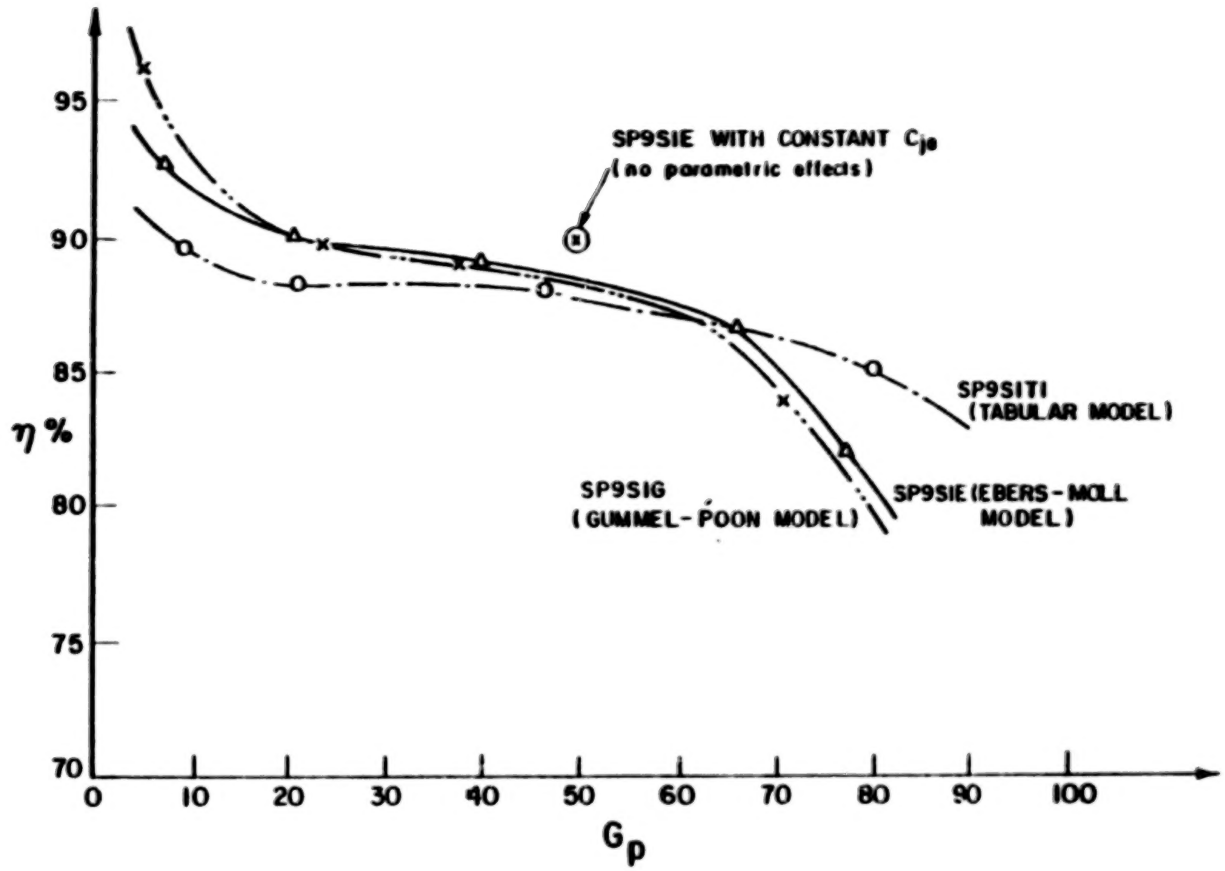


Fig. 5 Comparison of Class C results using the three models generated by BIPOLE and used in the WATAND non-linear network analysis program. The last letter of each name, E, G or T, refers to the model used i.e. Ebers-Moll, Gummel-Poon or tabular, respectively.

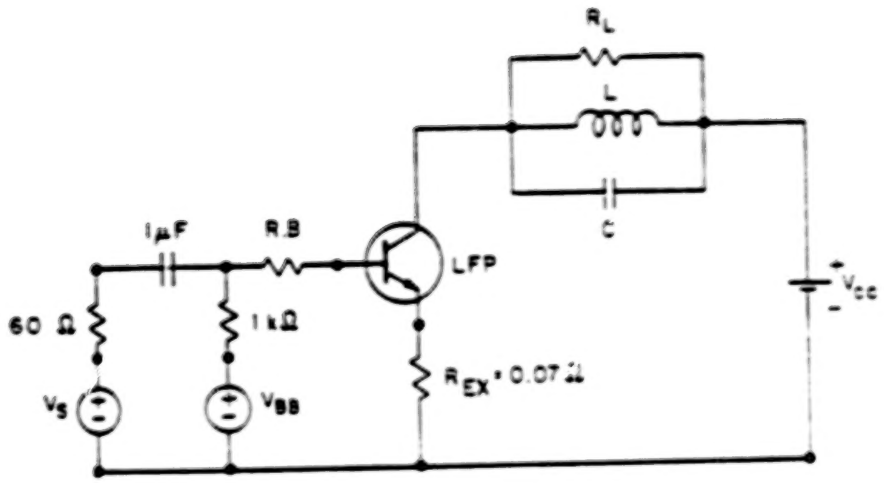


Fig. 6 Circuit used for the low frequency Class C laboratory and BIPOLE-WATAND simulation verification. Signal frequency 2.14 MHz, V_{cc} = 20 V, R_L = 500 ohms, R_B = 60 ohms, V_{BB} = 0 V, L = 4.27 μH.

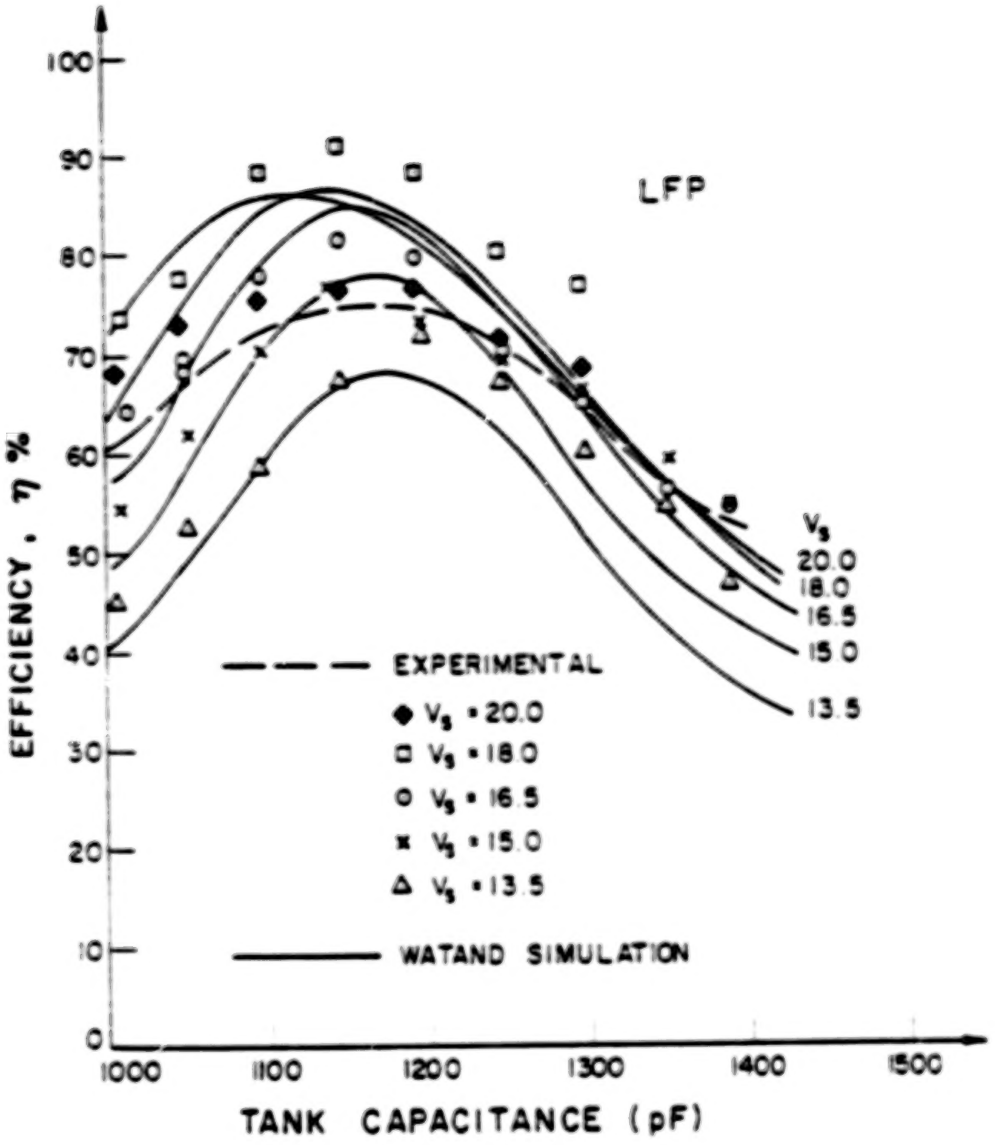
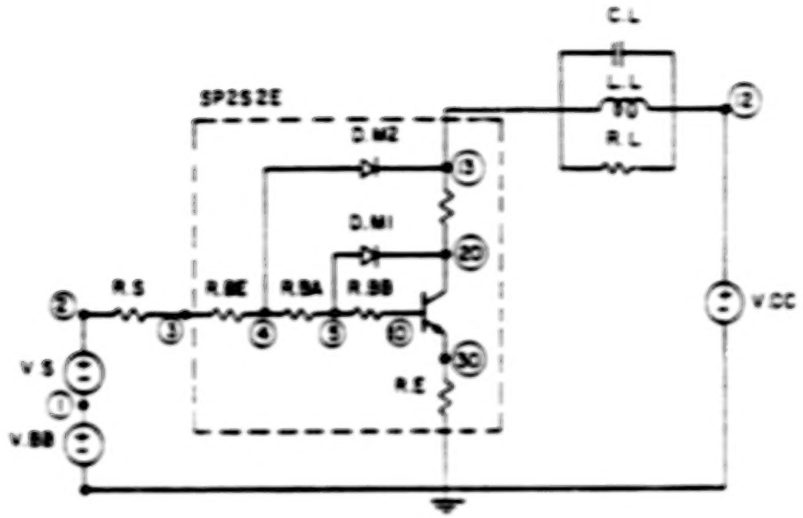


Fig. 7 Comparison of BIPOLE-WATAND computer simulation and laboratory measurements on a low frequency class C circuit. At the bias used this transistor (LFP) has f_t = 10 MHz (approx.), f_{mosc} = 70 MHz (approx.), (V_{cc} = 20 V). This represents therefore a crude scaling of the microwave case under study.



(a)

```
ST  SP252E    TRANSISTOR MODEL    JUL. 28, 1978        11:40:04
ST T = 27 DEGREES CELSIUS IKs  8.798E-03 VBCSB =  3.000E+01
SW
S.W1 CB   2.12E-16 CF   8.981E-01 CS   0.0         GO   4.298E-04  TE 300
+         LV   7.826E-01 BF   4.556E+00   1.415E+00   3.111E+00   5.975E-02
+         CE   1.027E-10   0.            1.017E+00   3.751E-01
+         CC   5.125E-12   0.            7.982E-01   4.634E-01
+         PT   6.926E-09   1.415E-00   8.786E-01  +1.800E+01 TS   6.517E-08
+ DA +100.  +50.  +20.  +10.  +5.  +1.  +.5  0  .2  .5  .6  .66  .7  .75  .8
+ .85  .9  .95  1.  1.05  1.1  1.15  1.2
S.W2 VB +100  0  2.272E-16  .898  12  0  RB  .06334  CC  3.000E+00  0.0  .7982  .4614
+ DA +100.  +50.  +20.  +10.  +5.  +1.  +.5  0  .2  .5  .6  .66  .7  .75  .8
+ .85  .9  .95  1.  1.05  1.1  1.15  1.2
S.W1 VB +100  0  2.272E-16  .898  12  0  RB  .0001  CC  5.000E+12  0.0  .7982  .4614
+ DA +100.  +50.  +20.  +10.  +5.  +1.  +.5  0  .2  .5  .6  .66  .7  .75  .8
+ .85  .9  .95  1.  1.05  1.1  1.15  1.2
#DA
R.S  2  3  .0001
R.BE  3  4  2.477E-2
R.BA  4  5  1.667E-2
R.BB  5  10  1.667E-2
S.W1  5  20
S.W2  4  10
V.W1  10  20  0V
R.E  30  0  2.206E-4
R.L  12  11  5.0E+11
R.C  12  11  5E+11
R.L  12  11  5
R.C  11  20  1.009E-1
V.CC  12  0  DC  15
V.BB  1  0  DC  0
V.S  2  1  SIN  1.3  2.495E9  0
#E
DC  DU  ALL  PR
** DE  4E-12 EN 8E-10 DU  V 11  0  2  9.0  5  V.CC    VB  0  60  CB  +1  1  PL
** **  1 WW  3 PR  V.B  DE  100 DU  V 11  0 VB  0  60  PL
DF  PR  V.S  DE  100 WW  2 DU  V 11  0  2  9.0  0  10  0  2  9.5  DF  33  PR  WA
#S
```

Fig. 8a Class C WATAND circuit

Fig. 8b WATAND file description of circuit with Ebers-Moll extended model.

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	1.2 OBJECTIVE	1-2	1/A13
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	3.3 AMPLIFIER CIRCUIT DESIGN RESULTS	3-5	1/B12
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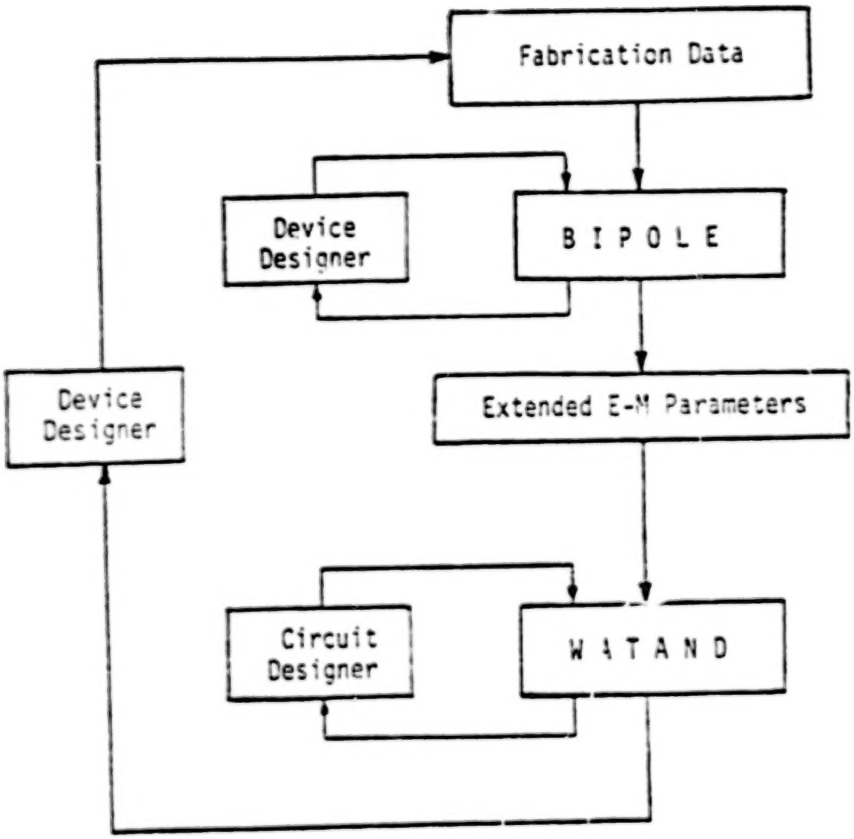


Fig. 9 Flow chart of general method used.

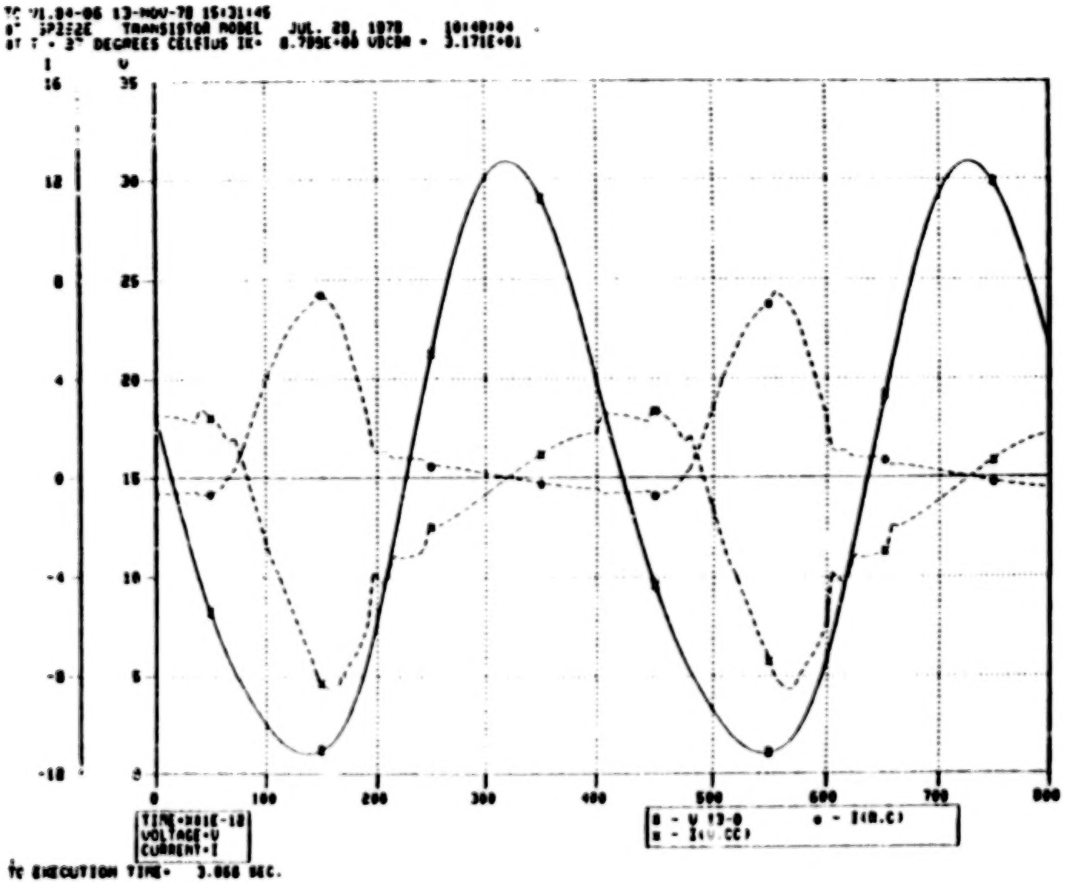


Fig.10 WATAND computed waveforms for the high-power non-saturated class C circuit in steady state, using SP2S2E transistor.

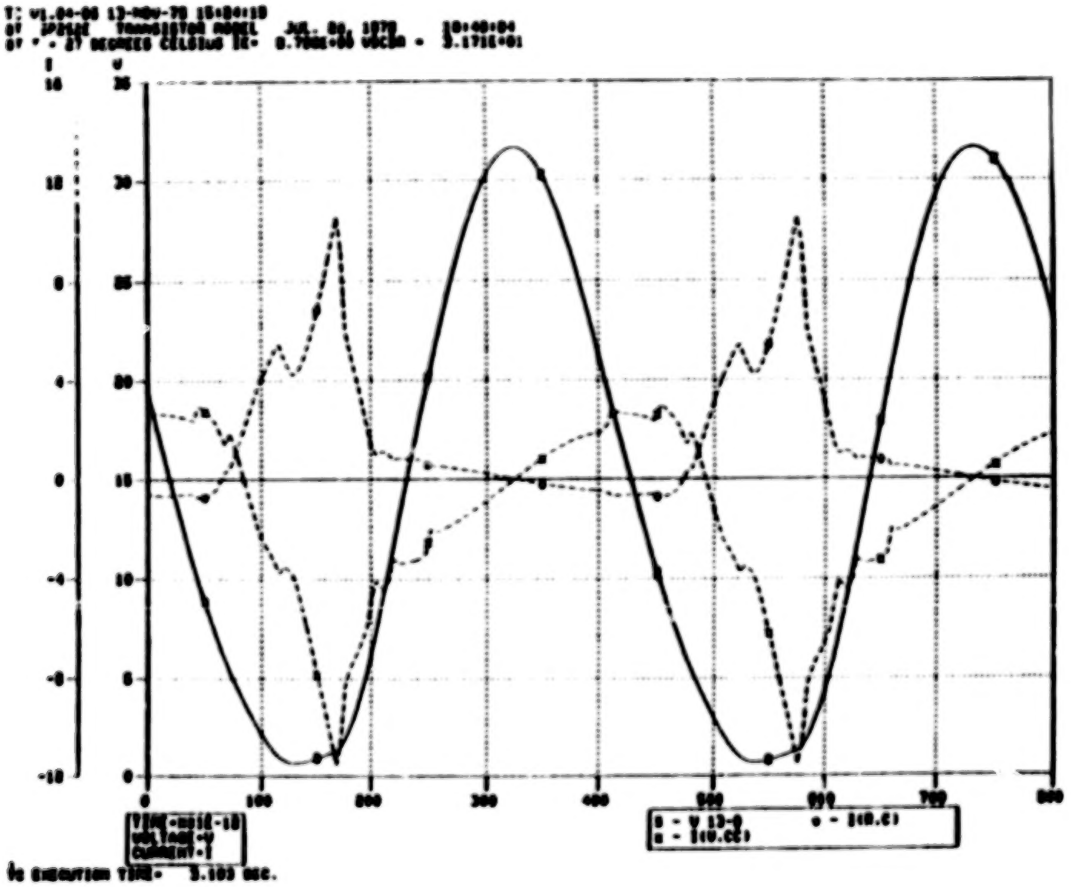


Fig.11 WATAND computed waveforms for the high-power saturated class C circuit in steady state, using the SP2S2E transistor.

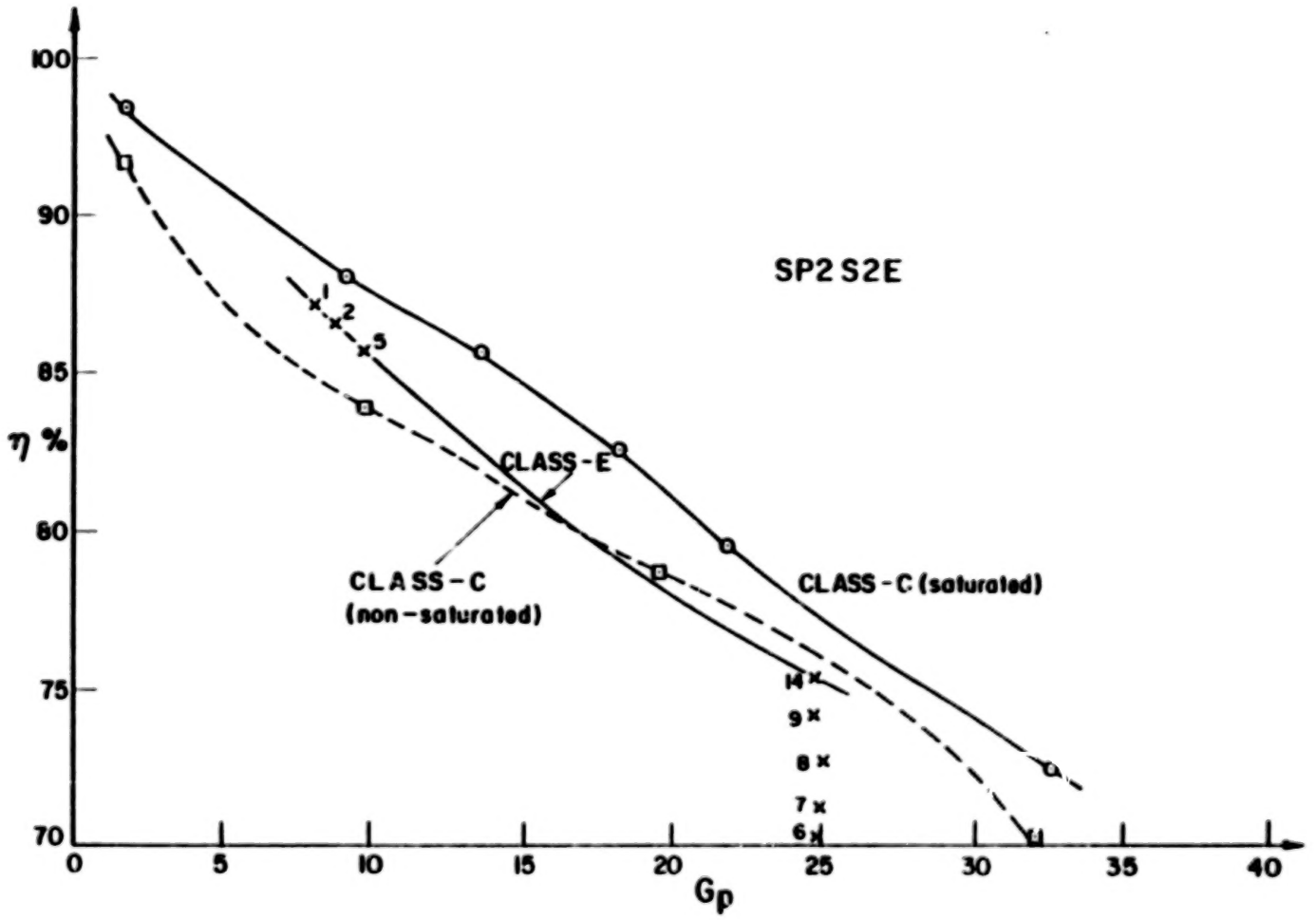


Fig.12 Comparison of BIPOLE-WATAND generated efficiency versus power-gain curves at 2.45 GHz and 27°C between high power (20 watts) Class C and Class E circuits using the silicon transistor SP2S2E. Both the normal (nonsaturated) and slightly overdriven (saturated) Class C cases are shown.

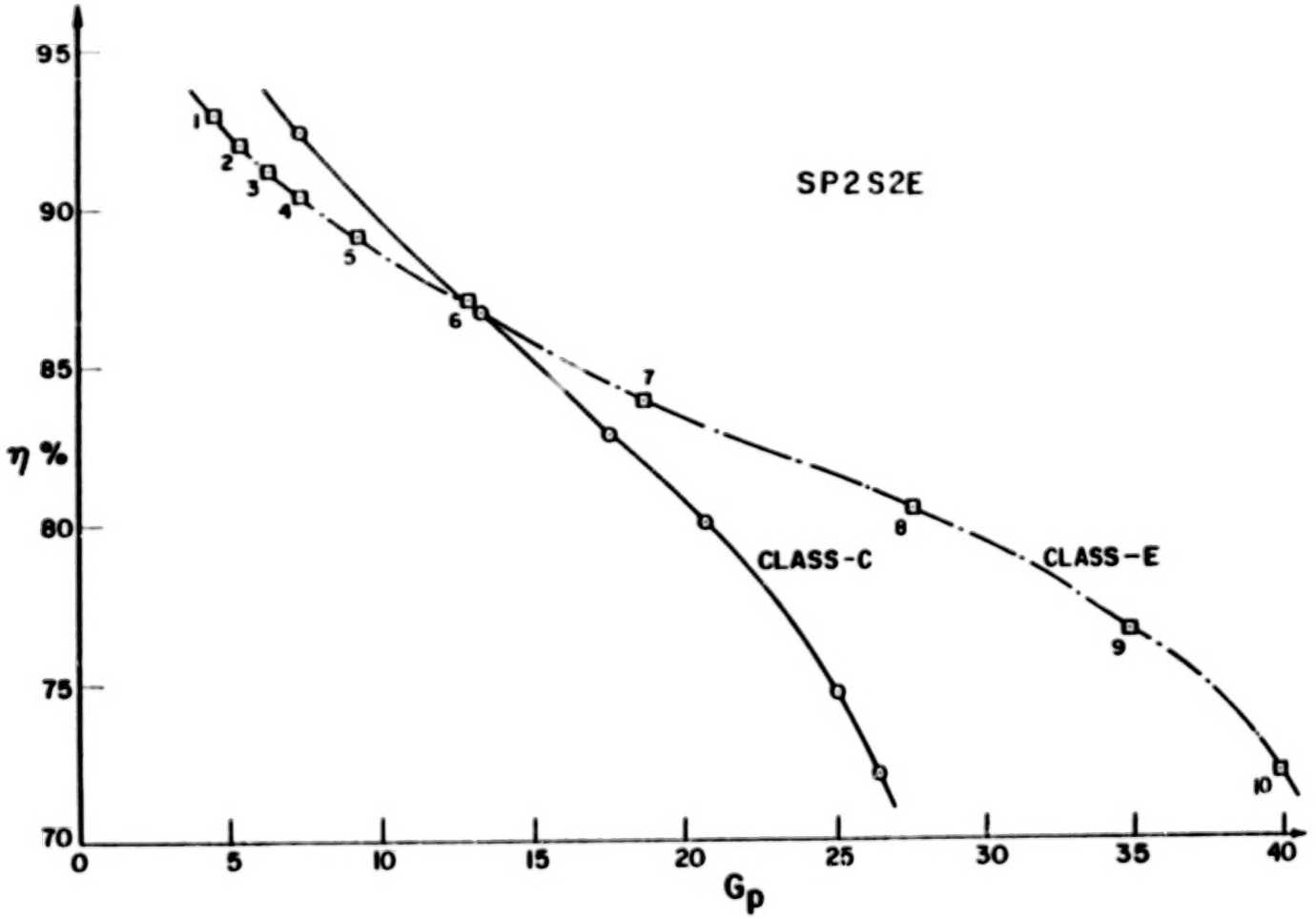


Fig.13 Comparison of BIPOLE-WATAND generated efficiency versus power-gain curves at 2.45 GHz and 27°C between low power (10 watts) Class C and Class E circuits. Only the 'saturated' Class C case is shown.

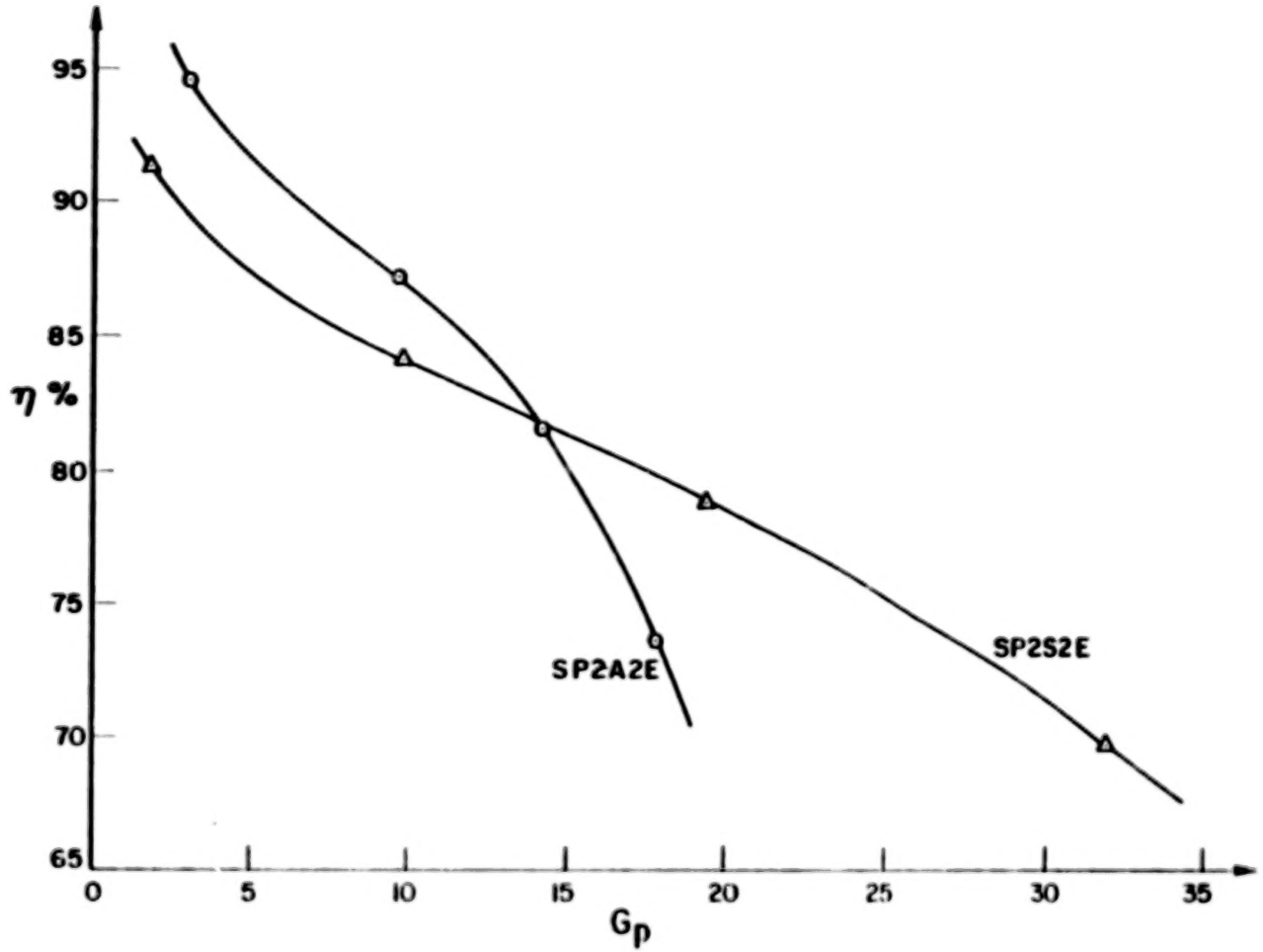


Fig.14 Comparison of BIPOLE-WATAND generated efficiency versus power-gain curves at 2.45 GHz and 27°C between the GaAs transistor (SP2A2E) and the silicon transistor (SP2S2E) in the high-power Class C (non-saturated) circuit with a load resitance of 5 ohm.

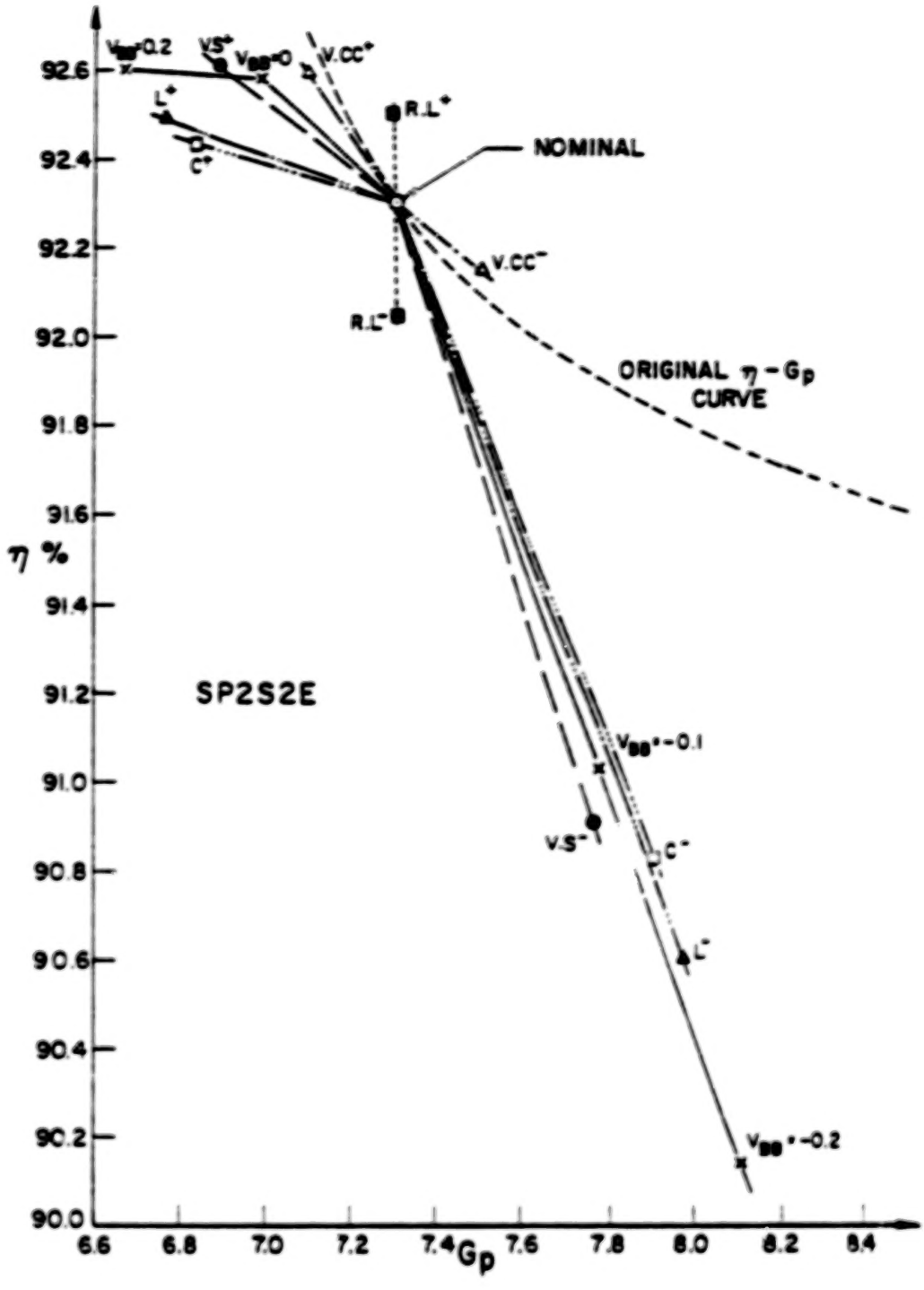
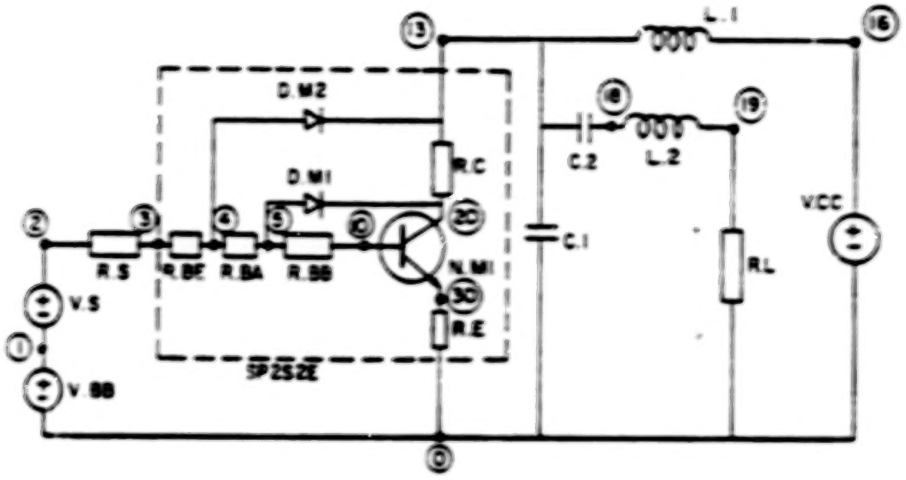


Fig.15 Low power (10 watts) saturated Class C sensitivity analysis with the SP2S2E transistor. Nominal values are:
V.S = 1.15 Volts, V.BB = 0 V, V.CC = 15 Volts, R.L = 12 ohm,
C.L = 56 pF, L.L = 60 pH. Variations are + 1% for
V.S, V.CC, C.L, L.L, V.BB is taken as -.2, -0.1, 0.1, 0.2.



(a)

```
t esp2s2e watand

#T SP2S2E  CLASS E CIRCUIT FOR 2.45GHZ OPERATION
#T BIPOLE GENERATED EBERS-MOLL PARAMETERS FOR WATAND USE
#T IK =  8.798E+00 VBCBR =  3.171E+01
#M
N.M1  IS  2.156E-16 IF  8.971E-01 IE 300.  CS  0.0
+ CC  4.299E-04 BR  7.847E-01 BF  4.524E+00  1.414E+00  3.159E+00  5.915E-02
+ CE  1.035E-10 0.0  1.017E+00  3.751E-01
+ CC  9.2E-12 0.0  7.982E-01  4.915E-01
+ FT  6.048E+09  1.414E+00  8.155E-01 -1.500E+01 TB  6.599E-08
+ SA -100. -50. -20. -10. -5. -1. -.5 0 .3 .5 .6 .65 .7 .75 .8
+ .85 .9 .95 1. 1.05 1.1 1.15 1.2
D.M2 VB -100 I1 2.156E-16 .8971 I2 0 RS .06336 CJ 3.12E-11 0.0 .7982 .4915
+ SA -100. -50. -20. -10. -5. -1. -.5 0 .3 .5 .6 .65 .7 .75 .8
+ .85 .9 .95 1. 1.05 1.1 1.15 1.2
D.M1 VB -100 I1 2.156E-16 .8971 I2 0 RS .0001 CJ 5.7E-12 0.0 .7982 .4915
+ SA -100. -50. -20. -10. -5. -1. -.5 0 .3 .5 .6 .65 .7 .75 .8
+ .85 .9 .95 1. 1.05 1.1 1.15 1.2
#DA
R.S 2 3 .25
R.BE 3 4 2.515E-2
R.BA 4 5 1.736E-2
R.BB 5 10 1.736E-2
D.M1 5 20
D.M2 4 11
N.M1 10 30 20
R.E 30 0 2.206E-8
R.C 11 20 1.009E-1
L.1 16 11 8.7N
C.1 11 0 0
C.2 11 18 8.6P
L.2 18 19 .71N
R.L 19 0 1.4
V.CC 16 0 DC  9.8
V.BB 1 0 DC .5
V.S 2 1 SIN 2.1 2.45E9 1.5
#E
DC OU ALL PR IP SE
TC DE 5E-12 EN 4.1E-10 OU V 11 0 I R.C   VB -10 40 IB -2 8 IP SS PL
SS IT 2 MP MM 8 PS V.S DE 100 OU V 11 0 VB 0 60 NO IP SS
DF PS V.S DE 100 NH 2 OU V 3 I R.S V 19 CO PA 0 1 4 0 IP SS
DF PS V.S DE 100 NH 2 OU V 19 I R.L V 16 I L.1 WA PA 0 0 0 0 IP SS
#S

R;
```

(b)

Fig.16a Class E WATAND circuit and Extended Ebers Moll model.

Fig.16b Class E WATAND file description of circuit (cf. entry 4 of table 2)

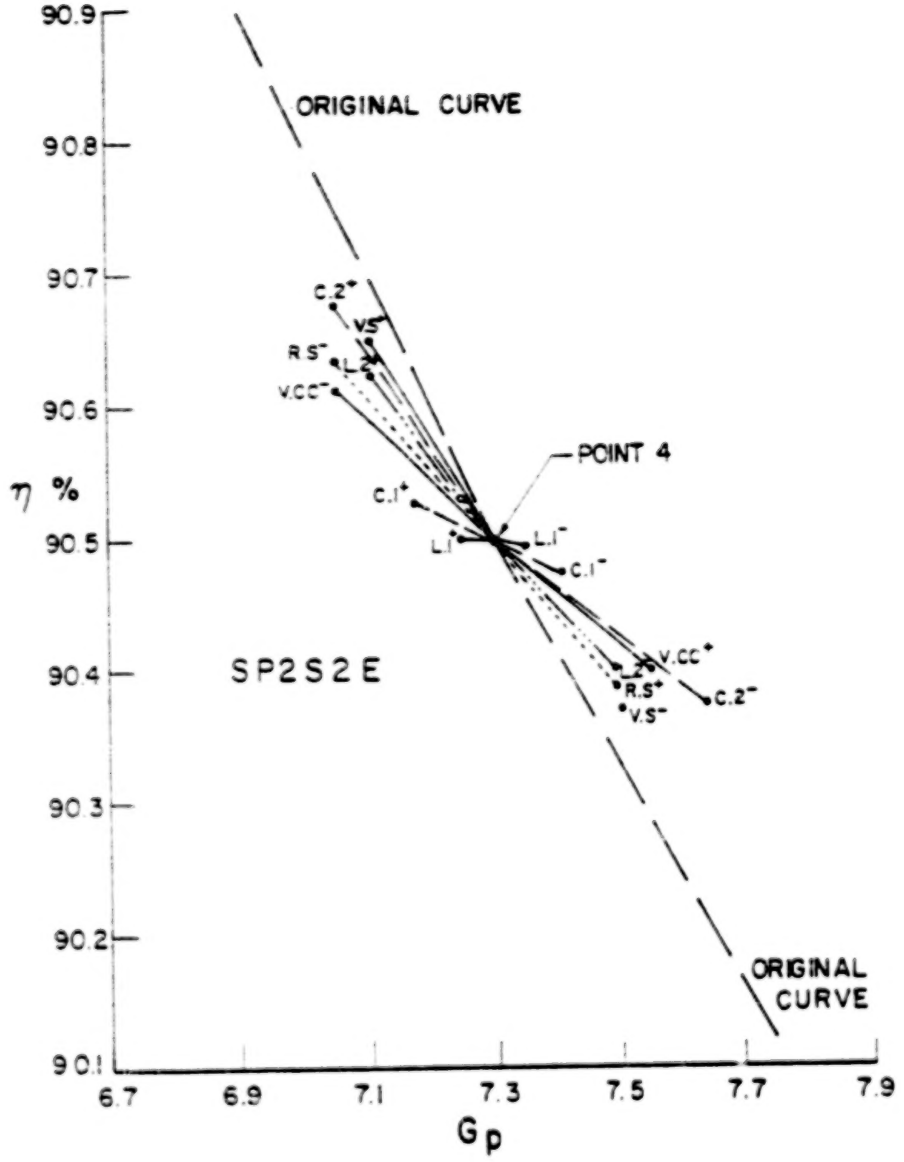


Fig.17 Low power (10 watts) Class E sensitivity analysis with the SP2S2E transistor. Nominal values correspond to entry 4 of table 2. R.S, R.L, V.CC, V.S varied ± 1%, C.1 ± 0.1 pF, L.1 ± 10%, V.B. ± 6% in small increments, C.2 ± 0.5%, L.2 ± 0.25%.

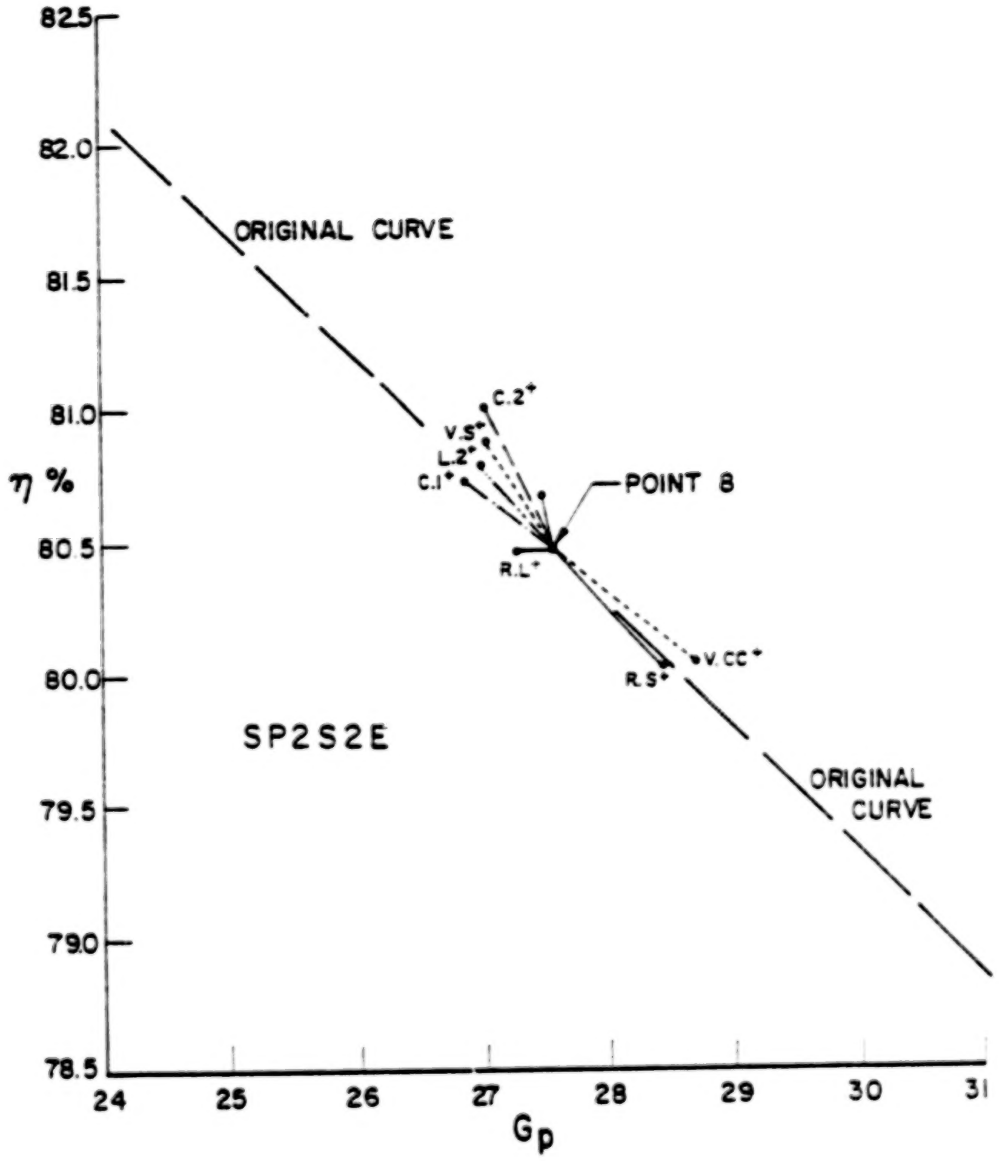


Fig.18 Low power (10 watts) Class E sensitivity analysis with the SP2S2E transistor. Nominal values correspond to entry 8 of table 2. R.S, R.L, V.CC, V.S, V.BB varied + 1%, C.2 + 0.5%, L.2 + 0.25% C.1 + 0.1 pF.

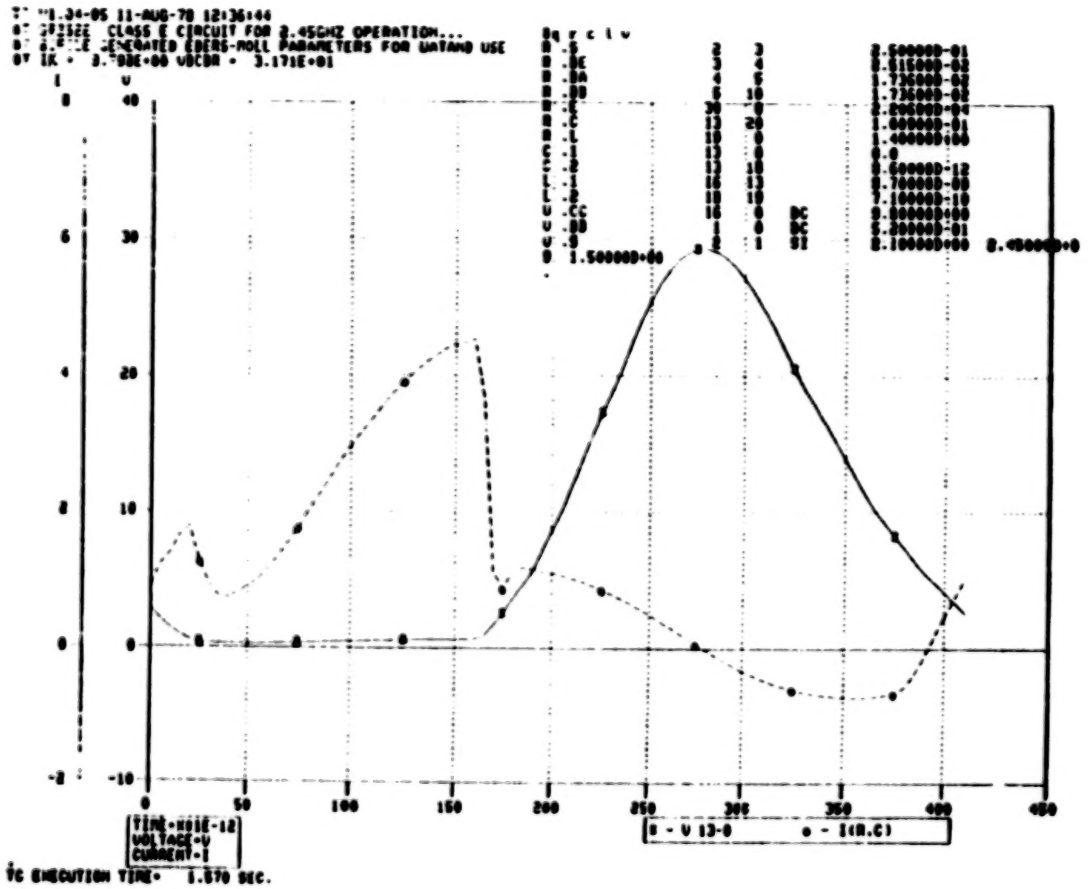


Fig.19 WATAND generated class E waveforms in steady state for v_{ce} and i_c (i_c into active transistor) for entry #4 of table 2.

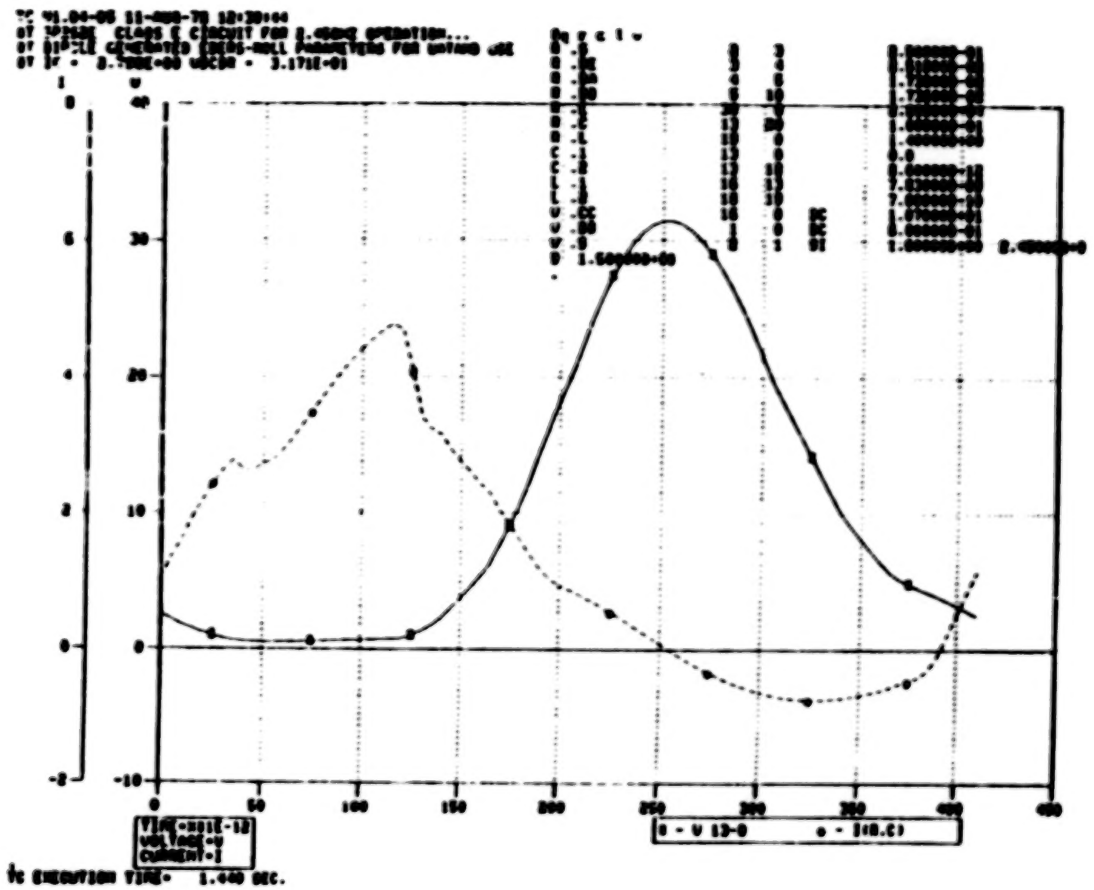


Fig.20 WATAND generated class E waveforms in steady state for v_{ce} and i_c (i_c into active transistor) for entry #8 of table 2.

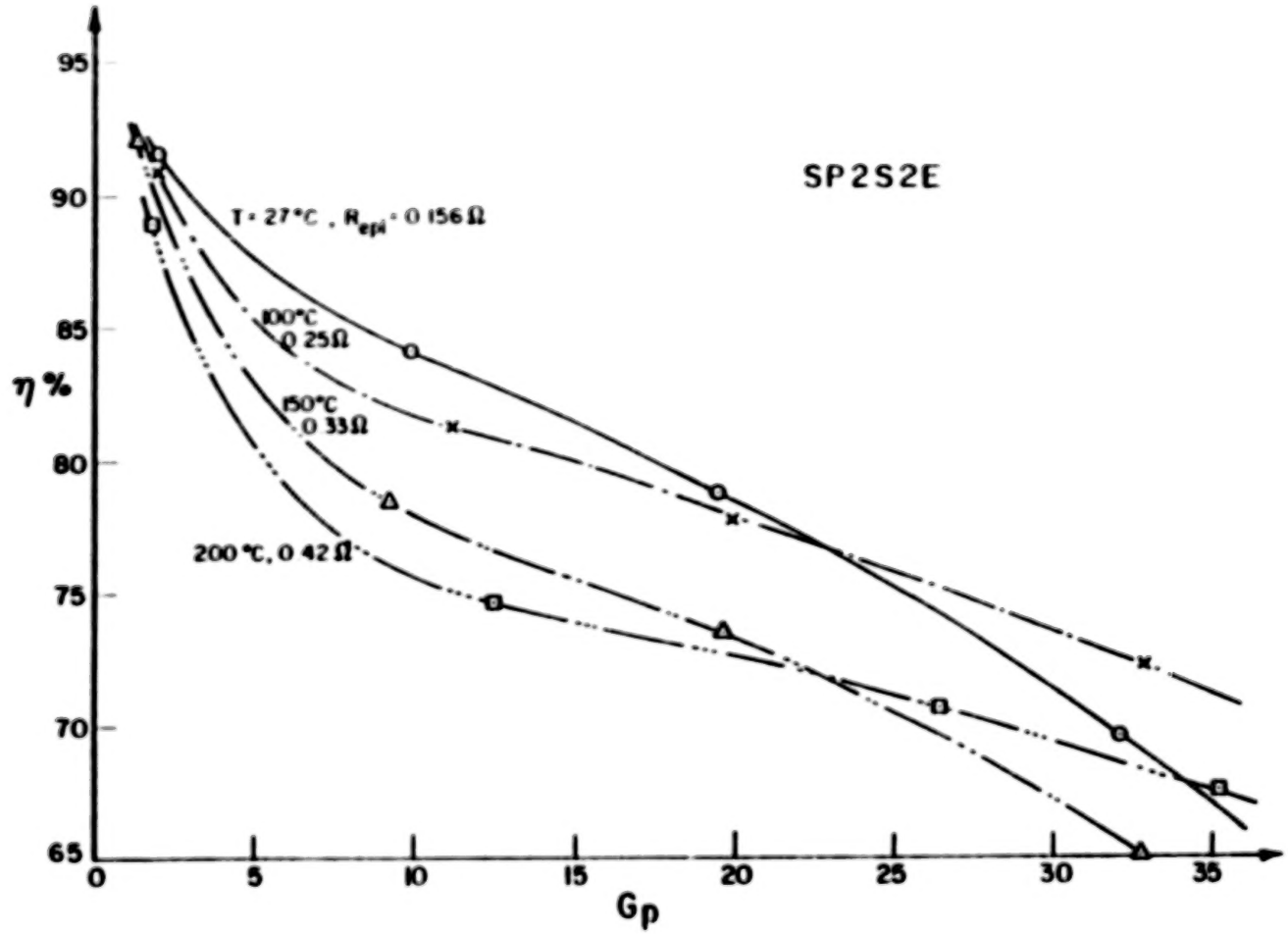


Fig. 21 Results of high temperature study using BIPOLE-WATAND for the silicon transistor (SP2S2E) at 2.45 GHz. Collector resistance is shown at each temperature.

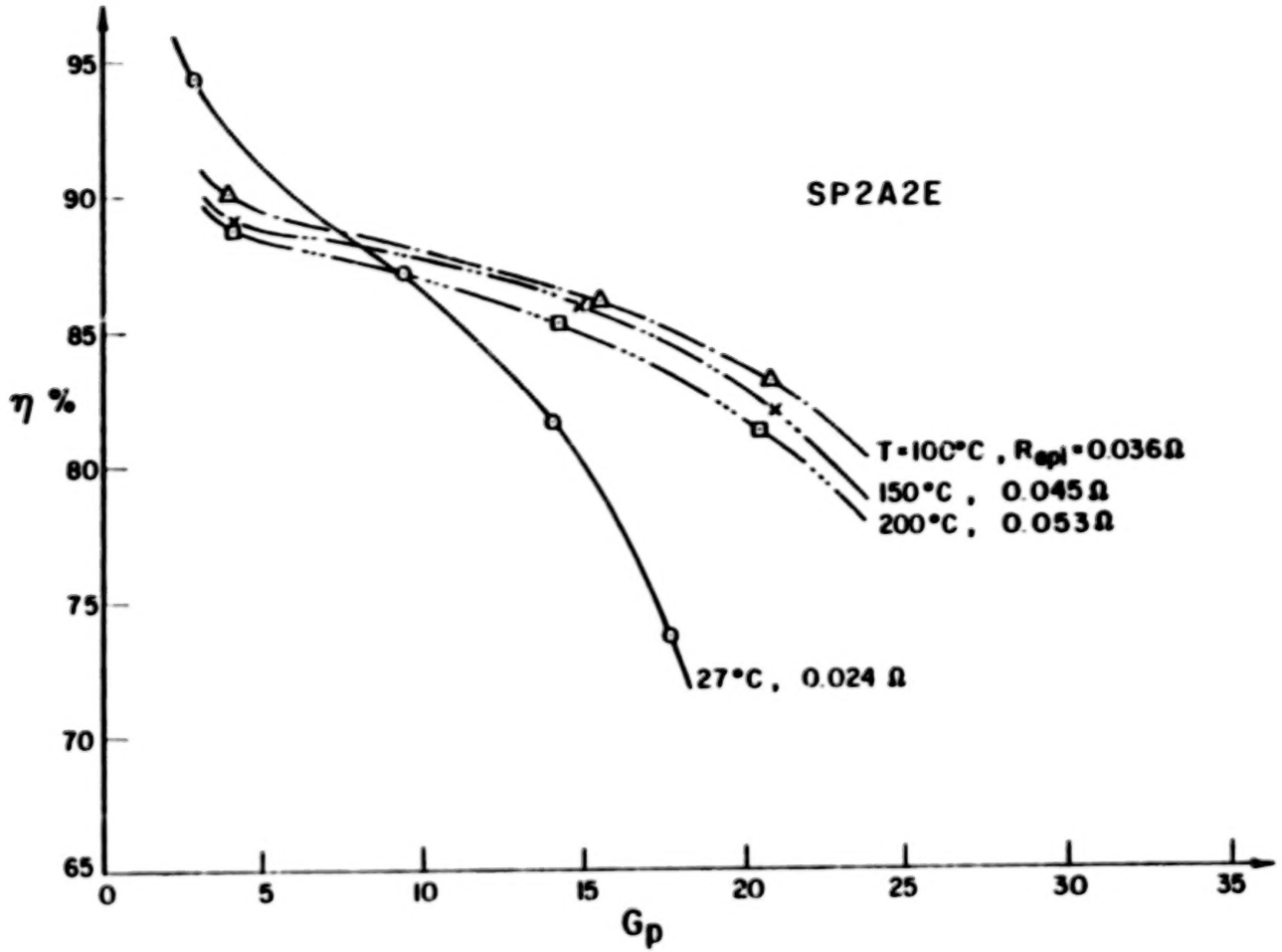


Fig.22 Results of high temperature study using BIPOLE-WATAND for the GaAs transistor (SP2A2E) at 2.45 GHz. Collector resistance is shown at each temperature.

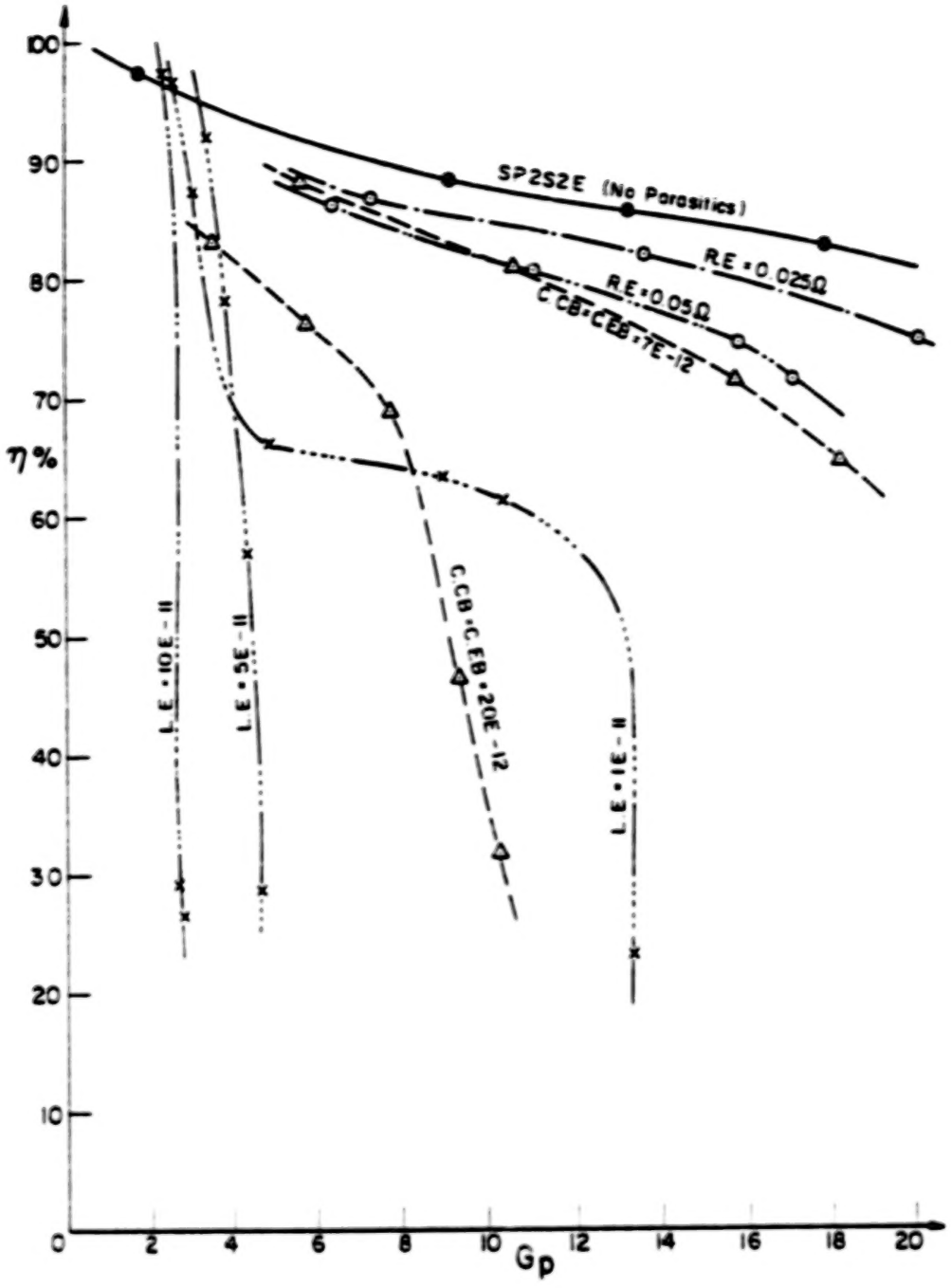


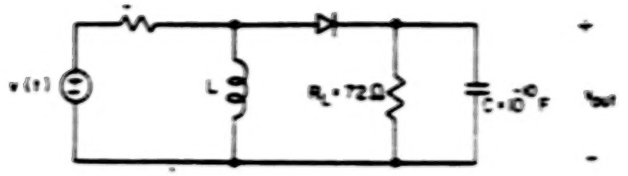
Fig.23 Effect of parasitics on performance of SP2S2E (silicon) transistor using WATAND (2.45 GHz).

R.E. is the emitter thermal ballast resistance (ohms)

L.E is the series emitter inductance (H)

C.CB is the external collector-base (bonding-pad) capacitance

C.EB is the external emitter-base capacitance.



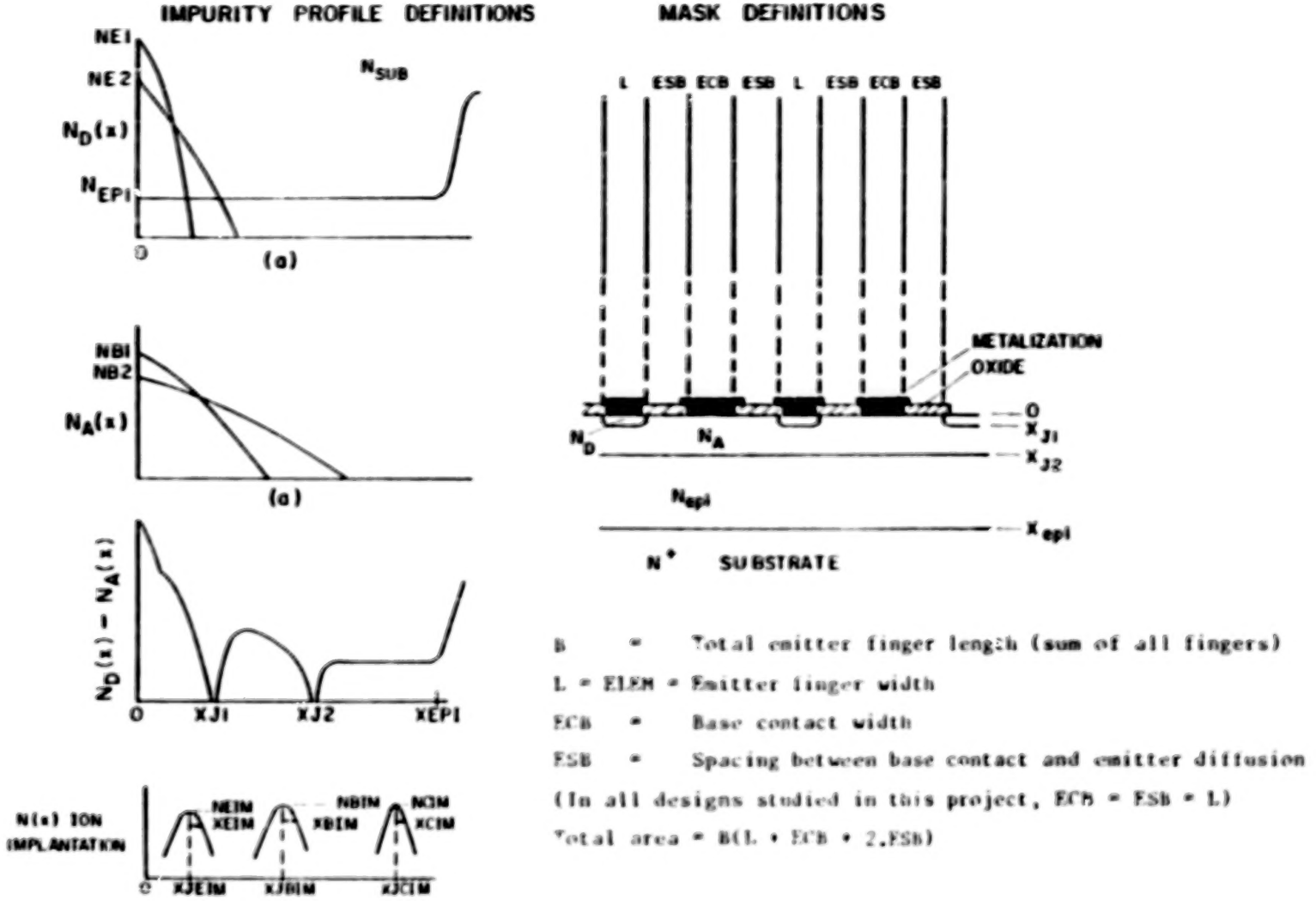
(a)

DIODE	Max. J_n (A/cm^2)	Area (cm^2)	N_D (cm^{-3})	W_{epi} (μm)	R_D (Ω)	C_J (PF)	I_S (A)	V_B (V)	L (H)	η%
GaAs										
D_1	10^3	0.5×10^{-3}	5.8×10^{15}	6.0	0.3	12.5	1E-10	-110	1.6E-9	74.3
D_2	10^4	0.5×10^{-4}	5.8×10^{15}	6.0	3.0	1.25	1E-11	-110	16 E-9	72.2
D_3	10^3	0.2×10^{-3}	2.8×10^{16}	1.6	0.055	9.6	1E-10	- 34	1.3E-9	77.2
D_4	10^4	0.2×10^{-4}	2.8×10^{16}	1.6	0.55	0.96	1E-11	- 34	11 E-9	73.1
Si										
D_5	10^3	0.2×10^{-3}	2×10^{16}	1.6	0.24	8.0	1E-10	- 34	1.5E-9	73.9
D_6	10^4	0.2×10^{-4}	2×10^{16}	1.6	2.4	0.8	1E-11	- 34	14.5E-9	69.0
D_7	10^3	0.5×10^{-3}	4.2×10^{15}	5.5	1.5	10.0	1E-10	-110	2.0E-9	65.1
D_8	10^4	0.05×10^{-3}	4.2×10^{15}	5.5	15.0	1.0	1E-11	-110	19.0E-9	51.9

(b)

Fig.24a Circuit used in the preliminary study for the rectenna diode.

Fig.24b Fabrication parameters and circuit performance computed with WATAND for 4 silicon and 4 GaAs diodes (all Schottky-barrier).



B = Total emitter finger length (sum of all fingers)

L = ELEM = Emitter finger width

ECB = Base contact width

ESB = Spacing between base contact and emitter diffusion

(In all designs studied in this project, ECB = ESB = L)

Total area = B(L + ECB + 2.ESB)

Fig.25 Plan and sectional diagrams of the transistors studied with profile data. Interdigitated or similar layout is assumed.

1 Report No	2 Government Accession No	3. Recipient's Catalog No
NASA CR-3323		

4 Title and Subtitle	5. Report Date
SATELLITE POWER SYSTEMS (SPS) CONCEPT DEFINITION STUDY VOLUME VI - IN-DEPTH ELEMENT INVESTIGATION	September 1980
	6. Performing Organization Code

7 Author(s)	8 Performing Organization Report No
G. M. Hanley	SSD 79-0010-6
	10 Work Unit No

9 Performing Organization Name and Address	11 Contract or Grant No
Rockwell International 12214 Lakewood Boulevard Downey, CA 90241	NAS8-32475
	13 Type of Report and Period Covered
12 Sponsoring Agency Name and Address	Contractor Report
National Aeronautics and Space Administration Washington, D.C. 20546	14 Sponsoring Agency Code

15 Supplementary Notes

Marshall Technical Monitor: C. H. Guttman
Volume VI of Final Report

16 Abstract

This document describes the effort undertaken under the leadership of Dr. D. Roulston, Department of Engineering, Waterloo University, Waterloo, Ontario Canada. This effort was accomplished under subcontract M8M8BNS-892055E to Space Systems Group of Rockwell International in support of the Solar Power System (SPS) study (NAS8-32475, Exhibit C, NASA/MSFC).

The goal of the study was to determine the fabrication parameters of GaAs MESFET solid-state amplifiers considering a power added conversion efficiency of at least 80% and power gains of at least 10dB. Operating frequency was to be 2.45 GHz although 914 MHz was also considered. Basic circuit to be considered was either Class C or Class E amplification. Two modeling programs were utilized. A BIPOLE program with an extended Ebers-Moll device model and a modified WATAND program to model the amplifer circuit.

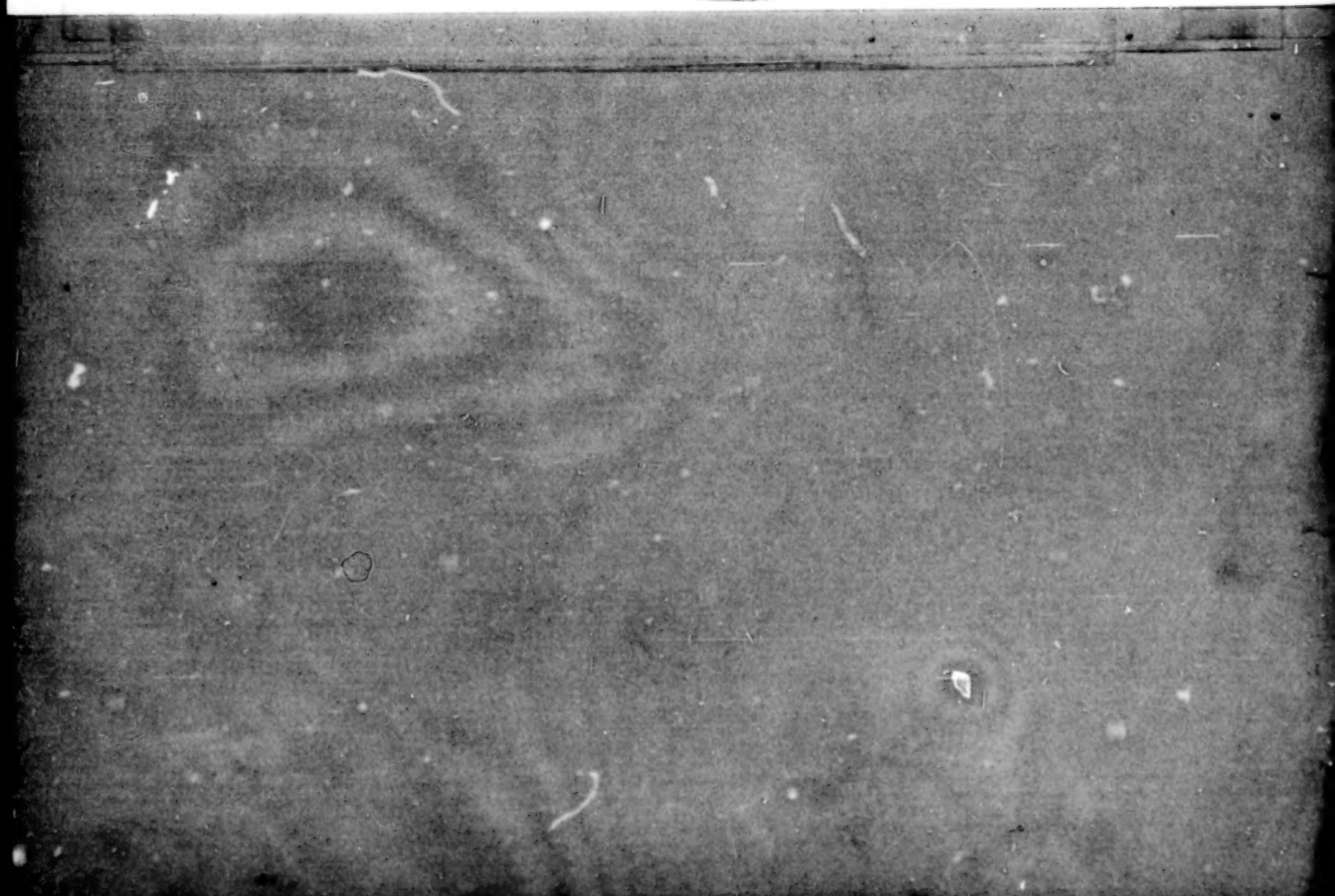
The data included in this report present the results of several computer calculations considering differing loads, temperatures, and efficiencies. Parametric data are presented in both tabular and plotted form.

17 Key Words (Suggested by Author(s))	18 Distribution Statement
Solid-state Amplifiers Amplifier Computer Simulation Satellite Power System SPS	Unclassified - Unlimited Subject Category 44

19 Security Classif (of this report)	20 Security Classif (of this page)	21 No of Pages	22 Price
Unclassified	Unclassified	107	A06

For sale by the National Technical Information Service Springfield Virginia 22161

NASA-Langley, 1980



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December 4, 1980